MODULE 6-ANALOG INTEGRATED CIRCUITS

CREDITS-4

COURSE CODE: EC 204

DATA CONVERTERS

- Converts one form of data into another form

There are two types of DATA converters-→ANALOG TO DIGITAL AND DIGITAL TO ANALOG

- The following are the **specifications** that are related to data conversions –

Resolution	accuracy	stability
Conversion Time	Linearity	settling time

RESOLUTION :smallest change in analog input voltage produced at the o/p of converter.

It depends on the number of bits that are used in the digital output. Mathematically, Resolution=$\frac{1}{2^n-1}$

8 bit converter -$\frac{Vfs}{2^8-1}$(for 8 bit converter)=39.2mV (resolution of 10V i/p range)

CONVERSION TIME:The amount of time required for a data converter in order to convert the data (information) of one form into its equivalent data in other form

ACCURACY:It is the maximum deviation b/w the actual converter o/p and ideal converter o/p

STABILITY:Performance of converter changes with temperature,age and power supply variations.So all the relevant parameters such as gain,linearity error etc must be specified over the full temperature and power supply range.

SETTLING TIME:time taken by the o/p to settle within a specified band ±0.5LSB of its final value.depends on switching time .Ranges from 100ns to 10μs.

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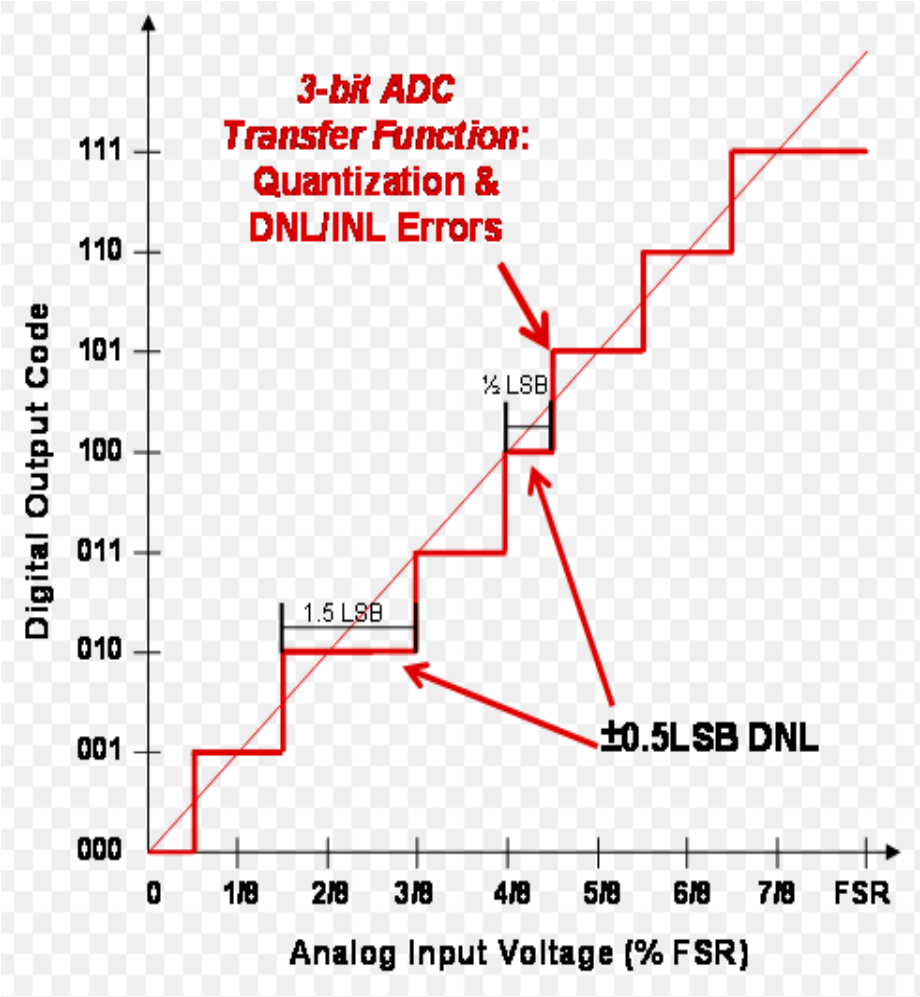
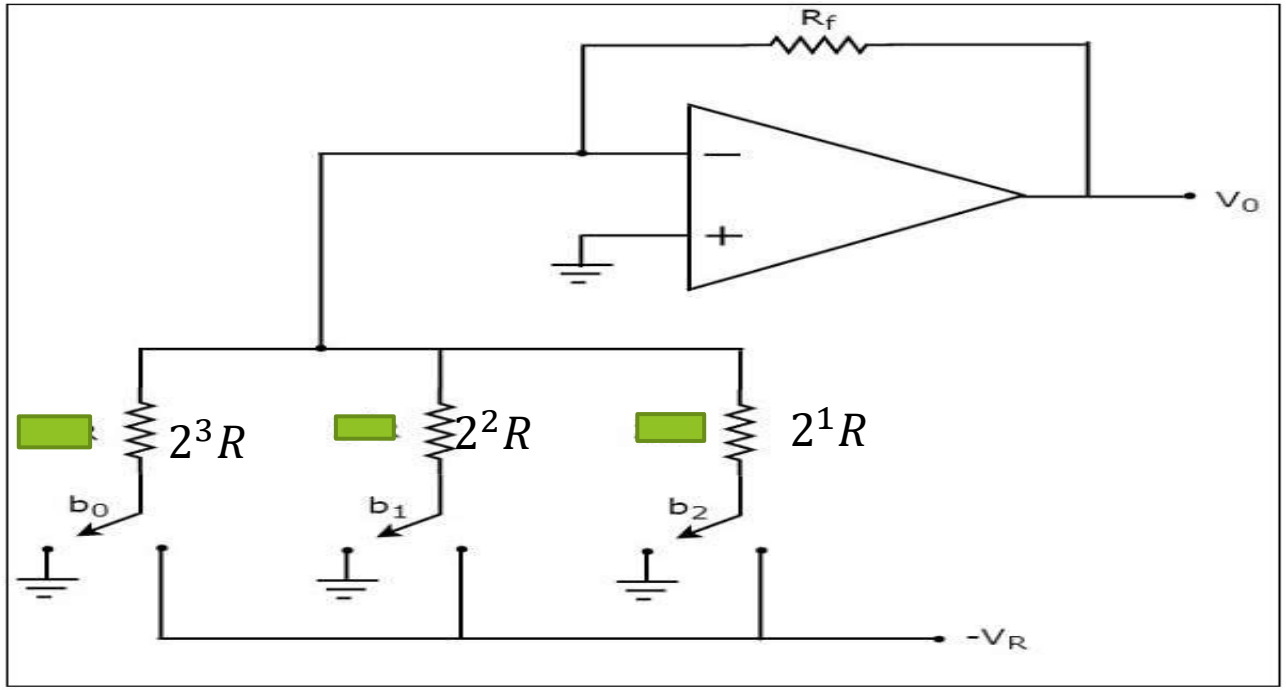
- LINEARITY: measure of its accuracy and tells us how close the converter o/p is to its ideal transfer characteristics. Ideal transfer curve for DAC is linear. Error is expressed as fraction of LSB increment or percentage of FSV. For good converter, error < ±0.5LSB



DAC-WEIGHTED RESISTOR TYPE

- A weighted resistor DAC produces an analog output, which is almost equal to the digital (binary) input by using **binary weighted resistors** in the inverting adder circuit.

The **circuit diagram** of a 3-bit binary weighted resistor DAC is shown in the following figure –



- Consider bits b2b1b0(b0-LSB and b2-MSB)
- the digital switches shown in the above figure will be connected to the negative reference voltage, -VR when the corresponding input bits are equal to ‘1’.
- According to the **virtual ground concept**, the voltage at the inverting input terminal of opamp is same as that of the voltage present at its non-inverting input terminal. So, the voltage at the inverting input terminal’s node will be zero volts.

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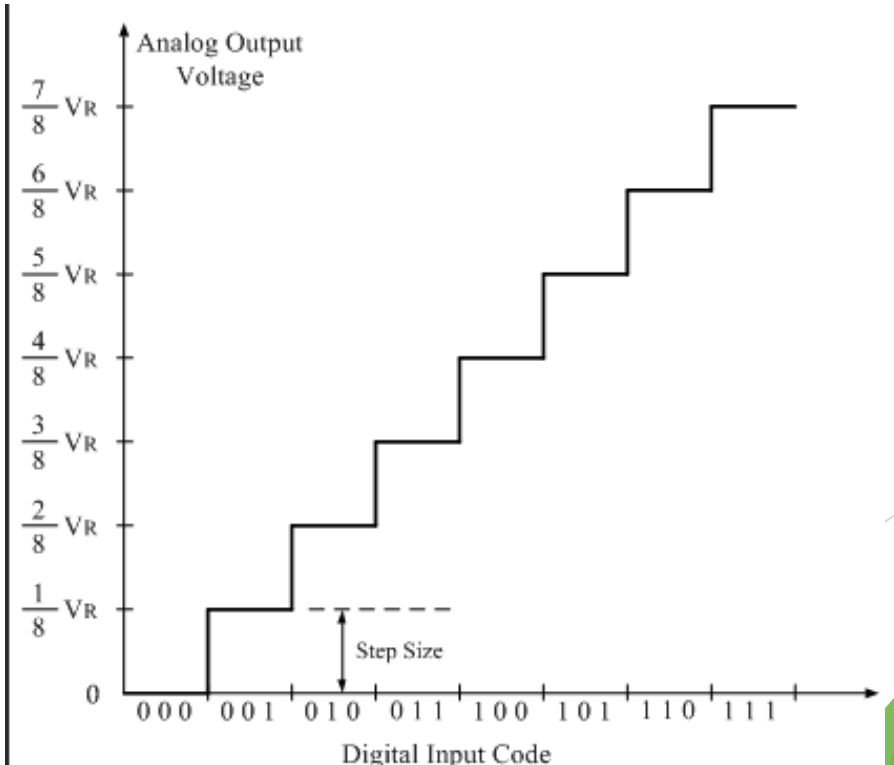
- $\frac{-Vr*b0}{2^3*R}+\frac{-Vr*b1}{2^2*R}+\frac{-Vr*b2}{2^1*R}=\frac{-V0}{Rf}$
- Vo=$\frac{Vr*Rf}{R}(\frac{b2}{2^1}+\frac{b1}{2^2}+\frac{b0}{2^3})$ Substitute R=Rf then Vo=$\frac{Vr*Rf}{Rf}(\frac{b2}{2^1}+\frac{b1}{2^2}+\frac{b0}{2^3})$ =$Vr(\frac{b2}{2^1}+\frac{b1}{2^2}+\frac{b0}{2^3})$

The **disadvantages** of a binary weighted resistor DAC are as follows –

- The difference between the resistance values corresponding to LSB & MSB will increase as the number of bits present in the digital input increases.
- It is difficult to design more accurate resistors as the number of bits present in the digital input increases for better resolution.
- Transfer characteristics of 3 bit DAC
- Operated as I to V converter

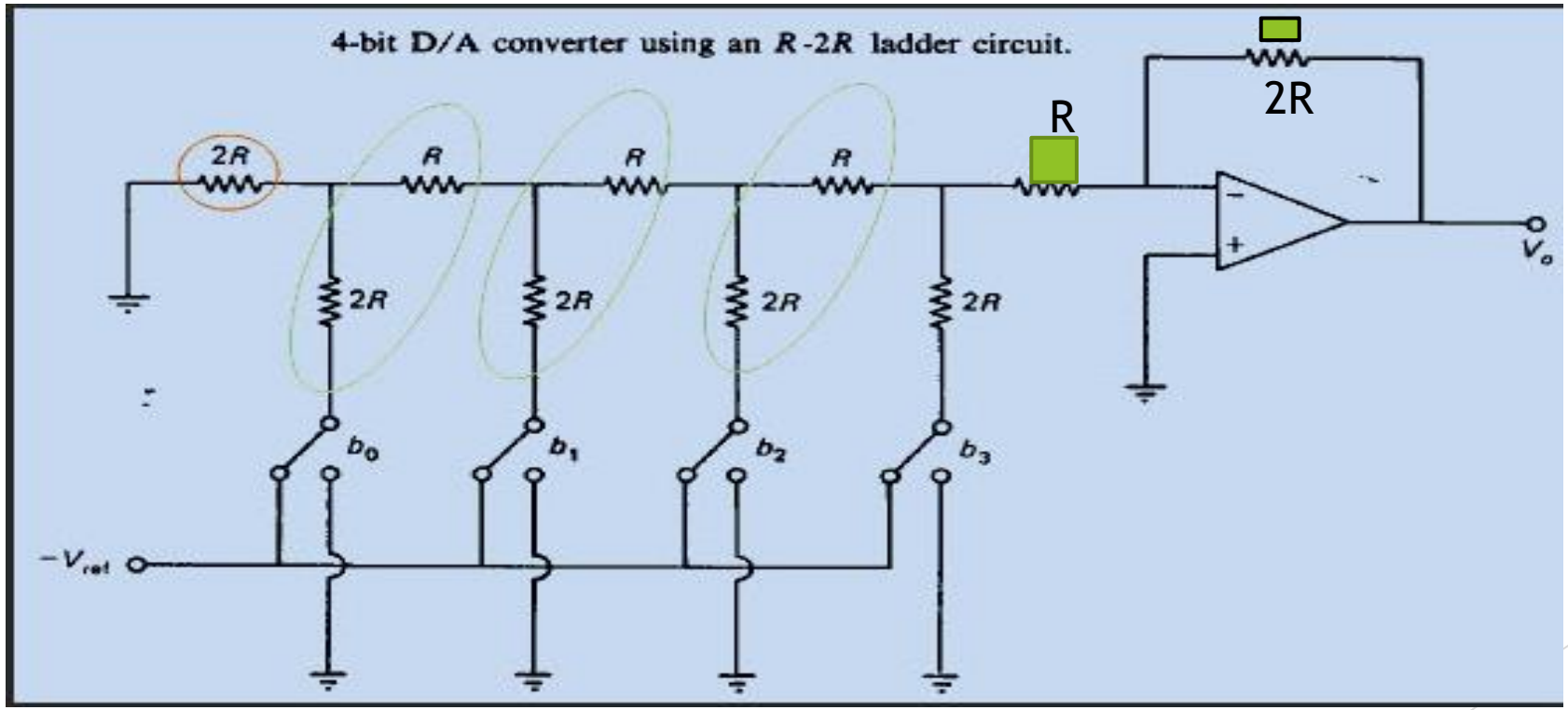


DAC-R-2R LADDER

- As wide range of resistors are used In weighted resistor type.This can be avoided by using R-2R ladder

Which uses only two type of resistors(R,2R)

$$Vo=\frac{-2R}{R} * simplified\ value\ acc\ to\ binary\ i/p$$



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Eg 1.Let us find the value of analog output voltage of R-2R Ladder DAC for a binary input, b2b1b0= 100.

As the i/p is 100, 2R||2R=R

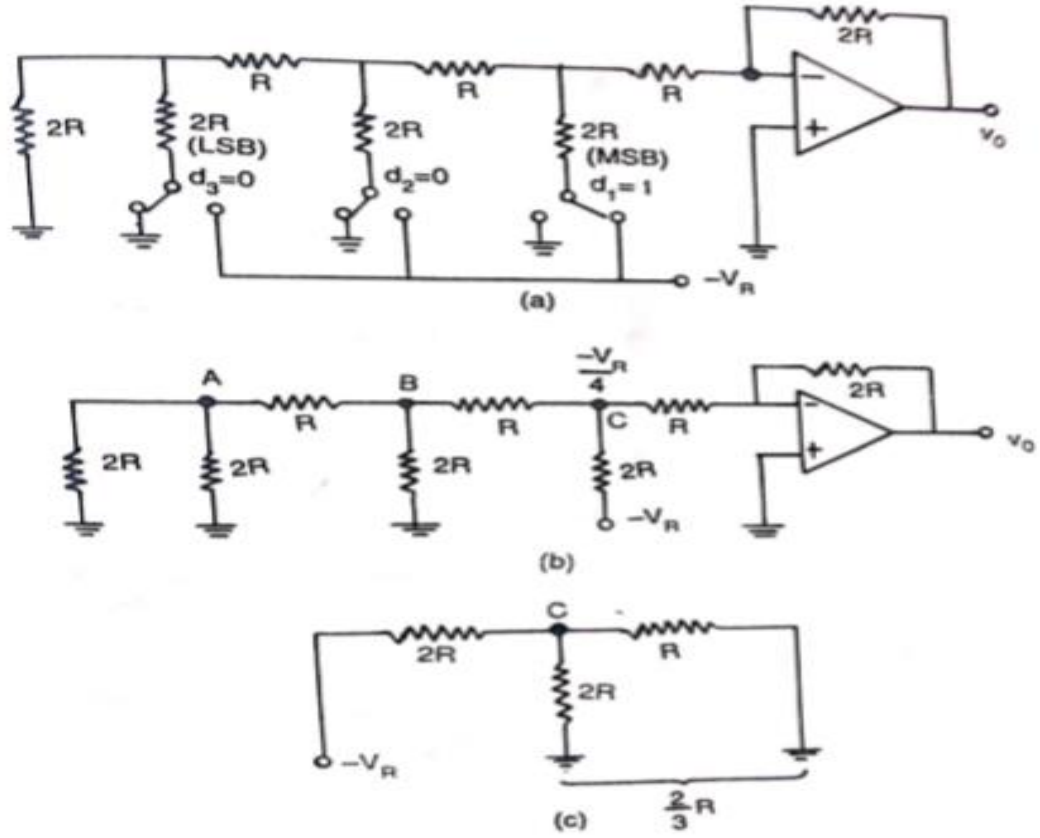
R+R=2R

2R||2R=R

R+R=2R and $\frac{2R*R}{3R}=\frac{2R}{3}$

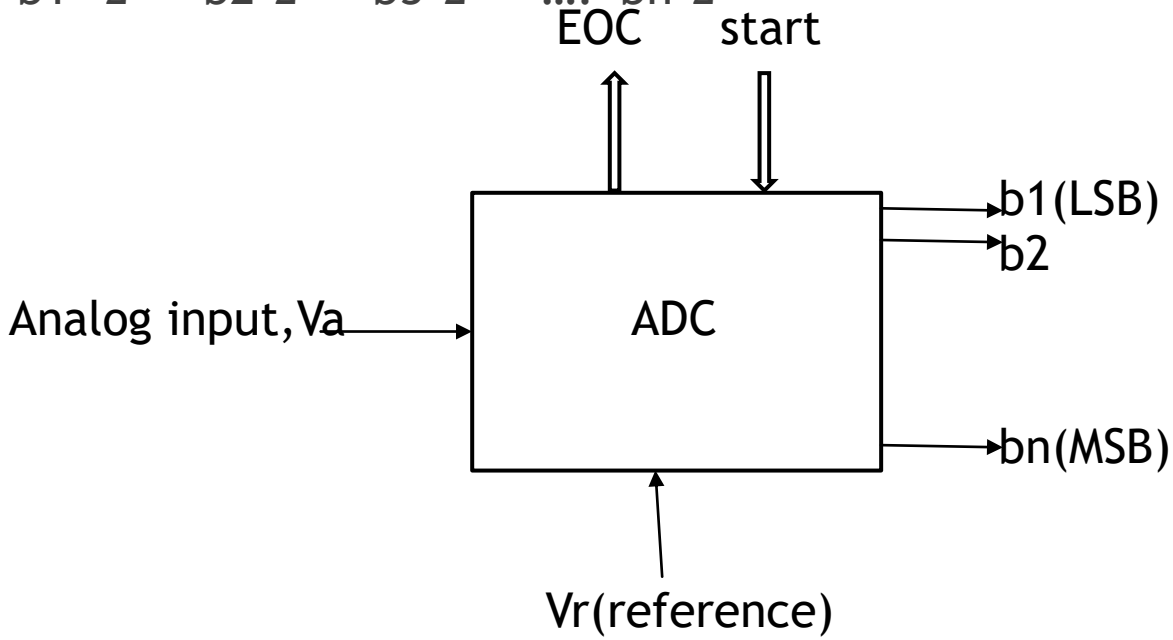
- Vo=$\frac{-2R}{R}(\frac{-Vr}{4})=\frac{Vr}{2}$

$$\frac{-V_R\left(\frac{2}{3}R\right)}{2R+\frac{2}{3}R}=-\frac{V_R}{4}$$



ADC

- Functions opposite to that of DAC.
- Accepts an analog input voltage Va and produces an o/p binary word b1b2…..bn
- D=b1$*\ 2^{-1}$+b2*2^{-2}+b3*2^{-3}+….+bn*2^{-n}



- 2 control lines:START input-when tostart the conversion

  EOC(end of conversion)-indicate the end of conversion
- 2 types of ADC-direct type and Integrating type
- Direct-given analog signal is compared with the internally generated eqwt signal

(a)Flash type(b)Counter type (c)Tracking (d) Successive approximation type

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- Integrating type-change the analog i/p signal to a linear function of time /frequency and to a digital code

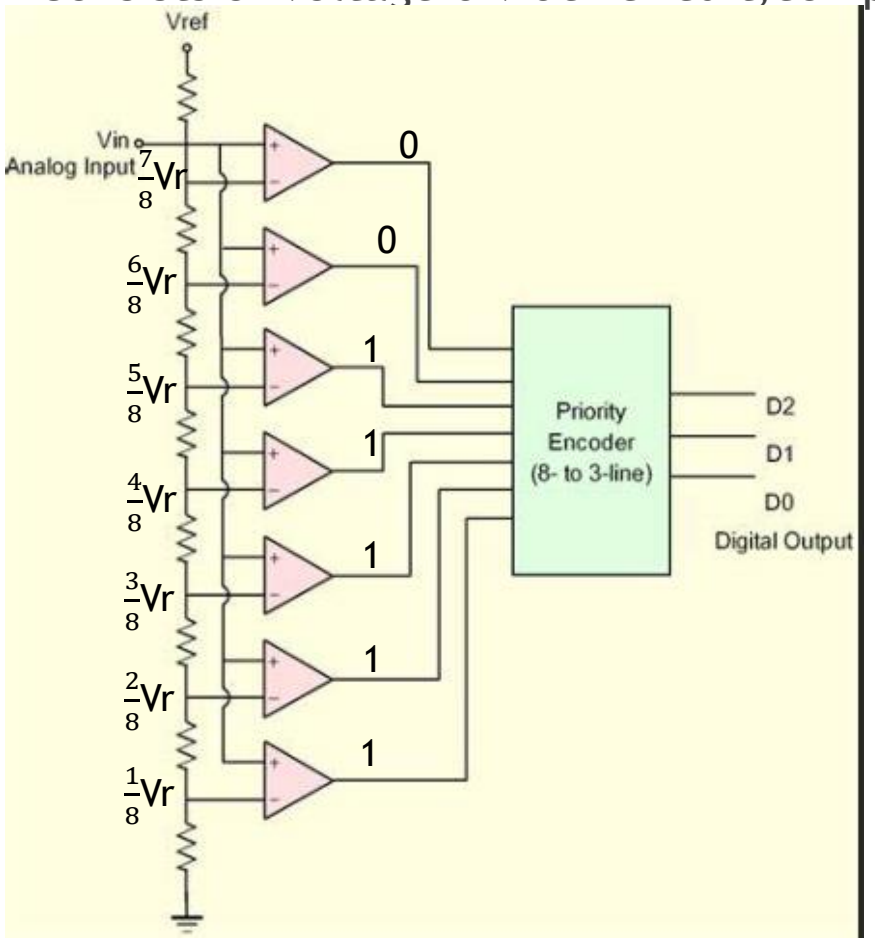
(a)Single slope(b)Dual Slope

- Successive Approximation Type is commonly used in applications like data loggers and instrumentation where conversion speed is high.Integrating type is also commonly used
- Successive approximation and Flash type is faster but less accurate than integrating type

ADC TYPE	FEATURES
Successive Approximation Type	Commonly used,complex,faster(high speed conversion),expensive,less accurate-DIRECT TYPE
Flash Type	Faster,expensive for high degree of accuracy,large power consumption-DIRECT TYPE
Counter type	Low speed-DIRECT TYPE
Integrating Type	Commonly used,More accurate,used in digital meter,panel meter,monitoring system

DIRECT TYPE ADCS

- COMPARATOR/FLASH TYPE ADC
- Simplest,fastest,expensive
- 2^n-1 comparators are required
- Fast conversion time due to parallel process
- Consists of voltage divider circuit,comparator,priority encoder



If	Output
Vin>Vref	High
Vin<Vref	Low

WORKING

- Reference voltage is connected to inverting terminal
- Analog input is connected to non inverting terminal
- Consider an analog i/p 5.5V and Vref 8V
- Voltage level at each points will be 7V,6V……and 1V.
- Most significant bit at which o/p of comparator is 1,corresponding bit number is the priority encoded value.Here for a 5.5V, encoded o/p is 101
- Consider for an analog value 3.3V ,Find the encoded value ?

Input voltage V_a	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $V_R/4$	0	0	0	0	0	0	1	1	0	0	1
$V_R/4$ to 3 $V_R/8$	0	0	0	0	0	1	1	1	0	1	0
3 $V_R/8$ to $V_R/2$	0	0	0	0	1	1	1	1	0	1	1
$V_R/2$ to 5 $V_R/8$	0	0	0	1	1	1	1	1	1	0	0
5 $V_R/8$ to 3 $V_R/4$	0	0	1	1	1	1	1	1	1	0	1
3 $V_R/4$ to 7 $V_R/8$	0	1	1	1	1	1	1	1	1	1	0
7 $V_R/8$ to V_R	1	1	1	1	1	1	1	1	1	1	1

Fig. 10.10 (c) Truth table for a flash type A/D converter

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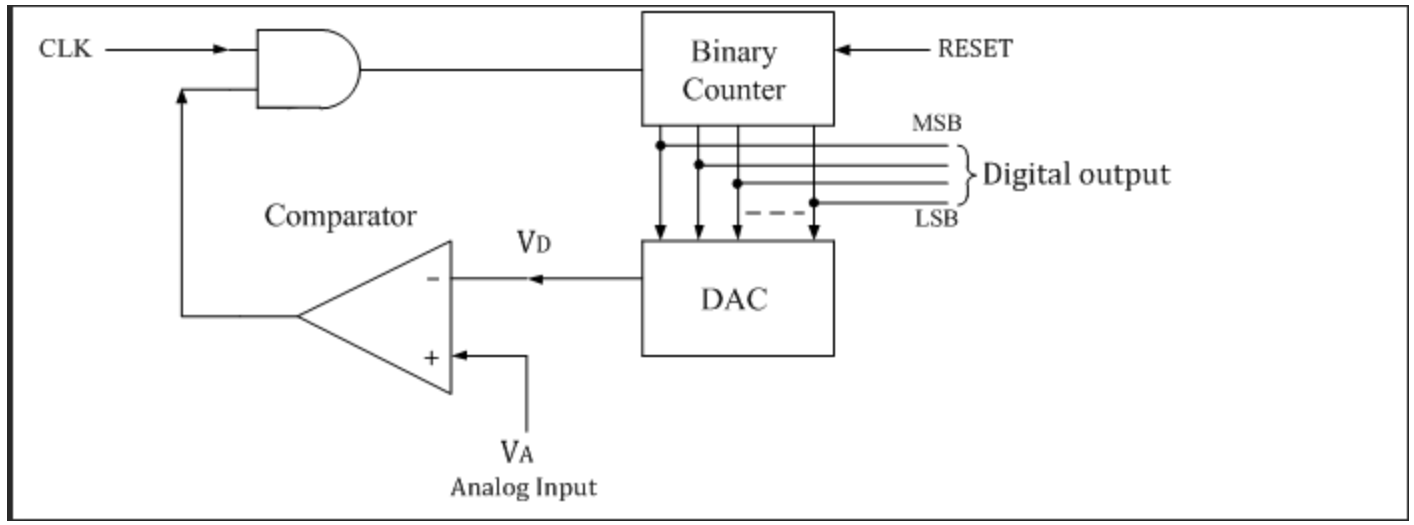
- Disdavantage:no:of comparators are double for each added bit.
- ie.2 bit ADC requires 3 comparators,3 bit ADC -7 and 4 bit ADC-15
- Complexity increases in priority encoder
- COUNTER TYPE ADC



- Comparator,AND gate,Binary counter,DAC
- Counter is reset to 0 by the reset pulse
- When the comparator o/p is high and on the application of clock,binary counter starts counting
- This is then fed to a DAC whose o/p looks like a staircase waveform
- DAC o/p is compared with the analog input using a comparator

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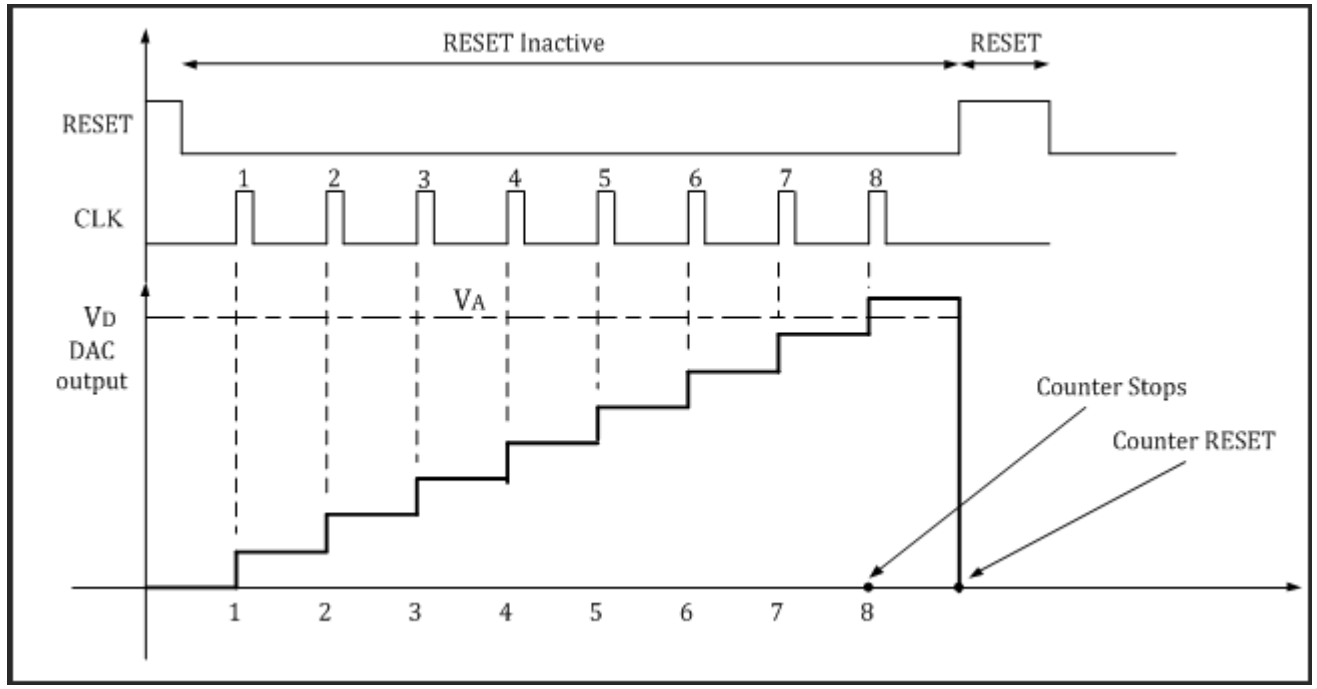
- If Va>Vd,o/p of comparator will be high and AND gate is enabled for the counter to count .
- If Va<Vd,o/p of comparator will be low and AND gate is disabled
- Counting action stops when Va≤Vd
- Counter frequency should be low to give sufficient time for the DAC to settle and comparator to respond
- Drawback:Low speed,conversion time is 2^n-1 clock periods
- Eg:for a 12 bit system with 1MHz clock frequency,counter will take $(2^{12}$-1)μs=4.095ms
- 

stair case waveform

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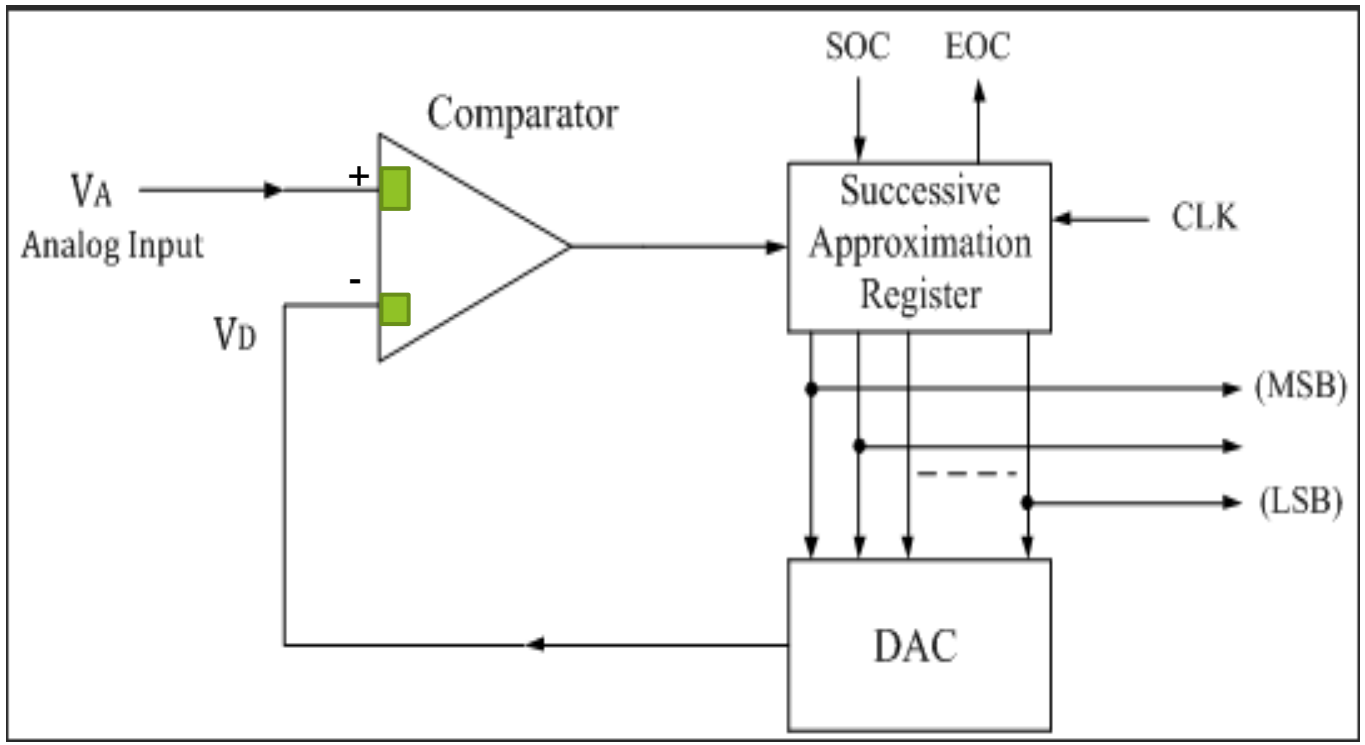
- SUCCESSIVE APPROXIMATION TYPE



- Efficient binary search strategy to complete n bit conversion in n clock periods(8 for 8)
- Time required for resetting SAR before conversion+time for performing conversion=total time
- No:of clock cycles =n(for conversion)+1(to reset before conversion)=n+1
- SAR(successive approximation register),DAC,comparator
- SAR-to find required value of each bit by trial and error

WORKING

- Initially SAR is set by the MSB,d1=1, and rest to 0 when clock is applied
- Trial code is 10000000
- o/p Vd of the DAC is compared with the analog i/p ,Va
- If Va>Vd,comparator o/p is 1 which implies 10000000 is less than the correct signal.
- MSB is retained at 1 and the next LSB is made 1 and tested.
- If Va<Vd then 1000000 is greater than correct digital representation
- So reset MSB to '0' and go on to the next LSB by making it 1
- This procedure is tested and for all subsequent bits on at a time, until all positions have been tested.

eg: Consider an analog input 36V and 8 bit SAR is used, 2^0, 2^1, 2^2..... 2^7

2^7 is set to 1→10000000 DAC comparator o/p will be 0 so MSB is reset to 0 and next bit is made 1

Then 64 is compared with 36 gives comparator o/p will be 0 so 00 and next bit is made 1

Then 32 is compared with 36 gives comparator o/p will be 1 so 001 and next bit is made 1

Then 48 is compared with 36 gives comparator o/p will be 0 so 0010 and next bit is made 1

Then 40 is compared with 36 gives comparator o/p will be 0 so 00100 and next bit is made 1

Then 36 is compared with 36 gives comparator o/p will be 1 so 001001 and next bit is made 1

Then 38 is compared with 36 gives comparator o/p will be 0 so 0010010 and next bit is made 1 and finally 00100100

Conversion sequence

- Eg:

Correct digital rep	Vd at different stages	o/p Y0
11010100	10000000	1
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	0

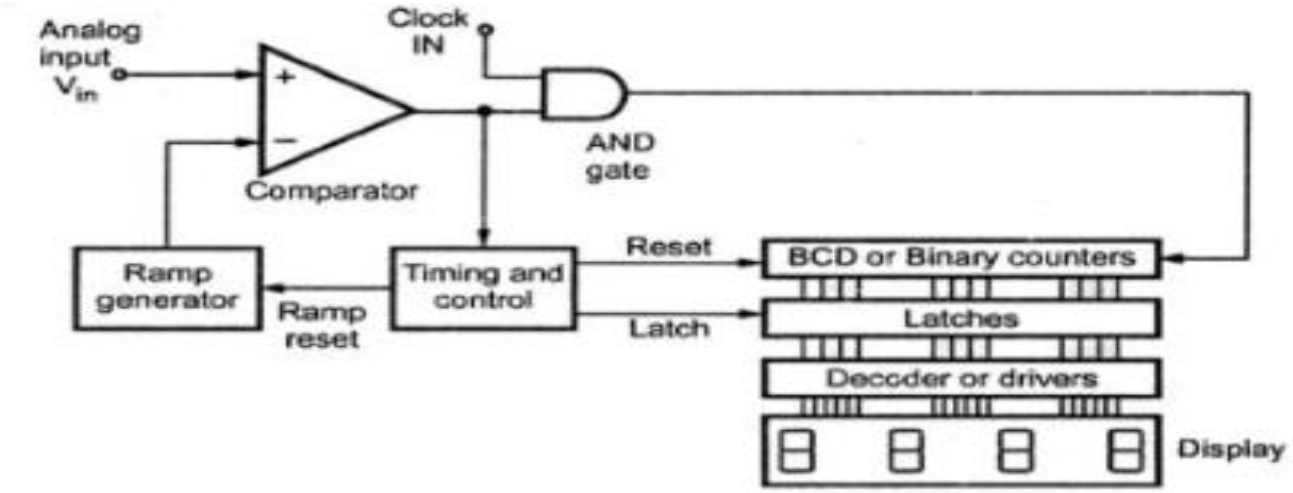
- Disadvantage:Complex design ,expensive
- Advantages:capable of high speed and reliable,medium accuracy,good trade off between speed and power

INTEGRATING TYPE ADC'S

- converts an unknown input voltage into a digital representation through the use of an integrator. The input voltage is computed as a function of the reference voltage, the time period.
- Converters of this type can achieve high resolution, but often do so at the expense of speed. For this reason, these converters are not found in audio or signal processing applications. Their use is typically limited to digital voltmeters and other instruments requiring highly accurate measurements.
- SINGLE SLOPE TYPE ADC

If conversion time is not important,single/dual slope type ADC.Technique is based on comparing the unknown analog i/p voltage with a reference voltage and increases linearly with time.

Time required for the reference voltage to reach the value of unknown analog i/p voltage is proportional to the amplitude of unknown analog i/p voltage.Time period can be measured using a digital counter.



Single slope ADC

Working

- Main circuit:Ramp generator(opamp based integrator circuit/DAC driven by a a binary counter)
- Reset from the control circuit is applied to the ramp generator
- Assume a positive analog input voltage Vi is applied at the non inverting i/p of the comparator
- When a RESET signal is applied to the control logic,BCD counter resets to 0 and ramp voltage begins to increase.As Vi is positive,comparator o/p is in HIGH state and allows the CLK to pass to the i/p of the counter through the AND gate and the counter is incemented.
- Process continues until the comparator o/p is high.When Va = ramp generator voltage,comparator o/p=0 and clk will not pass through the gate and counter operation is stopped.
- At that time, control logic generates a STROBE which latches and is displayed which is equivalent to the amplitude of analog input voltage.
- Disadvantage:
- due to component value errors and clock errors
- Change in C and R due to temperature affect the integrated o/p and introduce error
- Drift in clock frequency also causes errors

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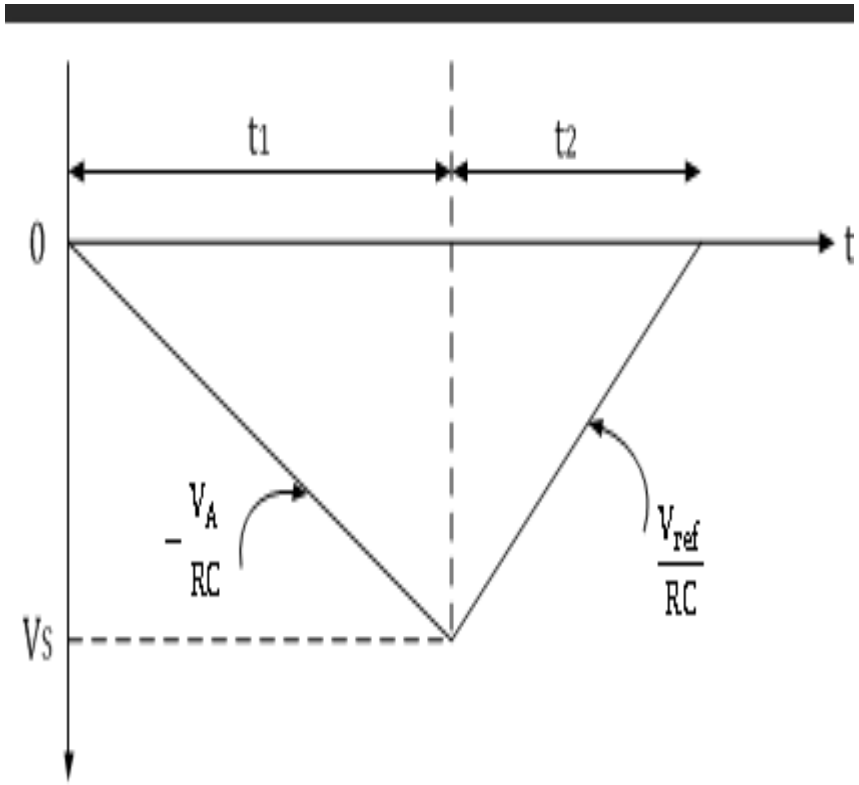
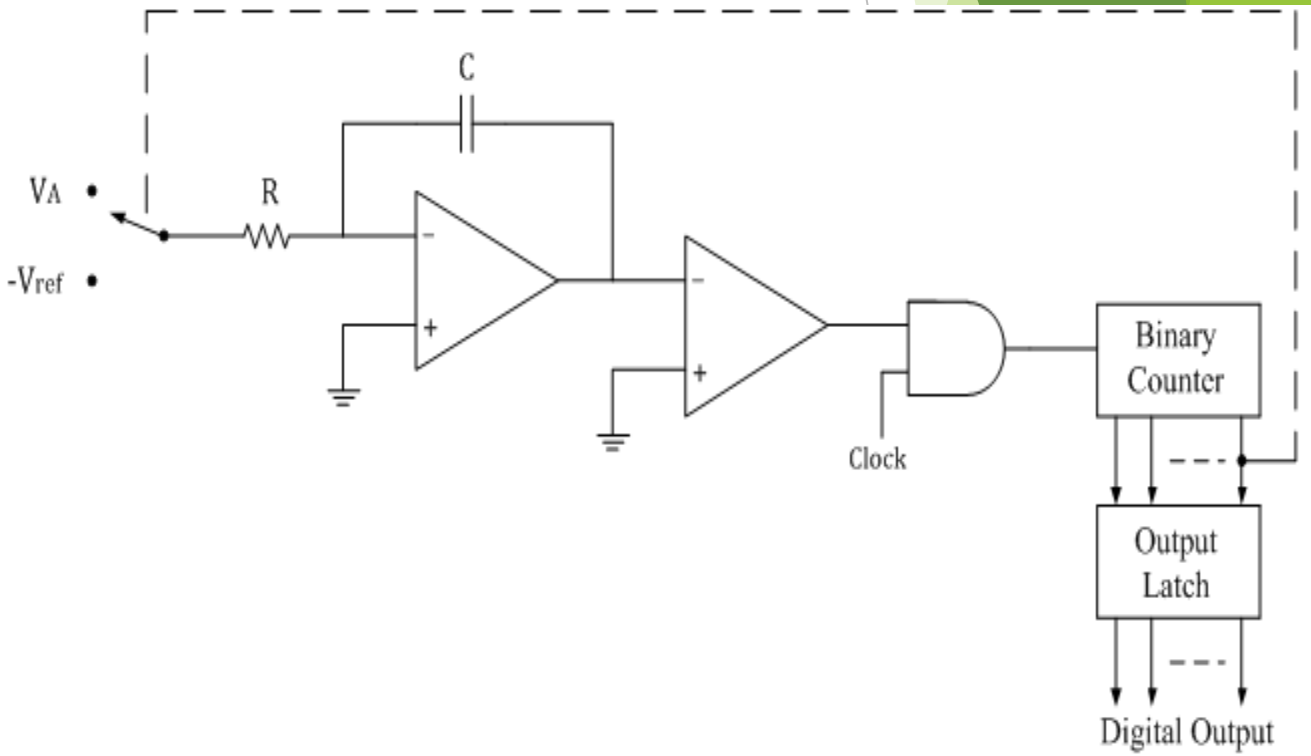
DUAL SLOPE TYPE ADC

- Unknown input voltage is applied to the input of the integrator and allowed to ramp for a fixed time period(t1) .
- Then a known reference voltage of opposite polarity is applied to the integrator and is allowed to ramp until the integrator output returns to zero(t2)
- Integrator generates two different ramps, one with an unknown i/p and another with a known reference voltage –Vr. So called dual slope.



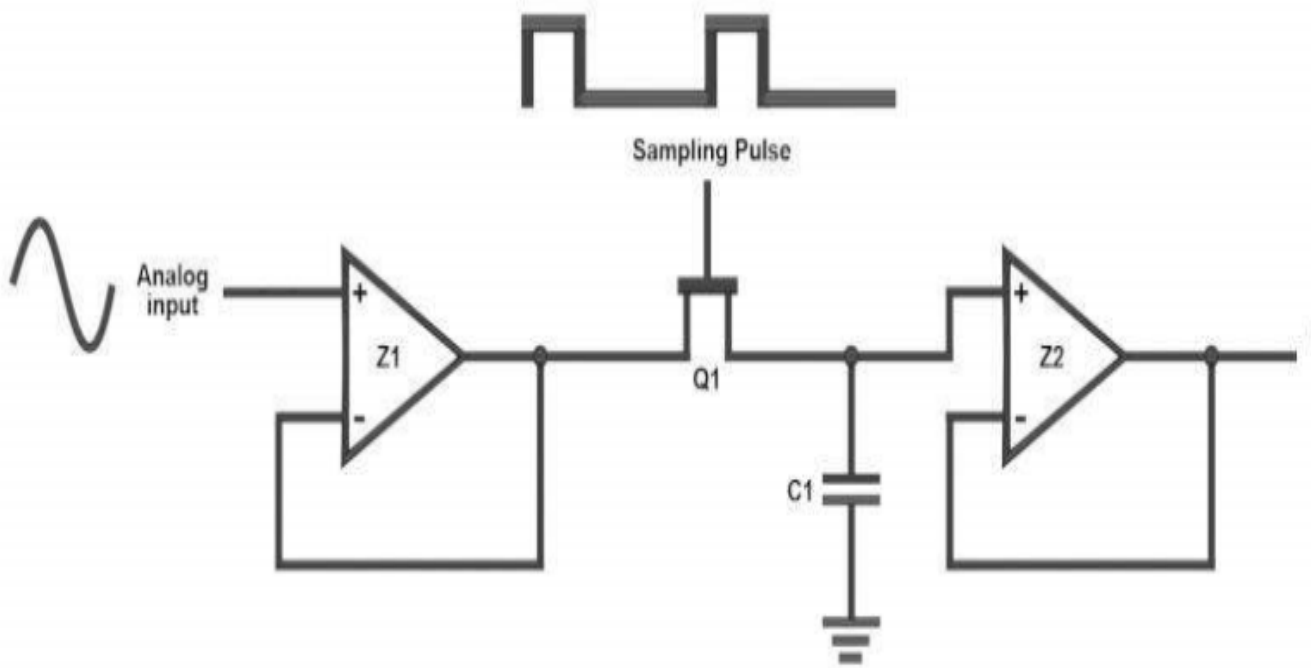


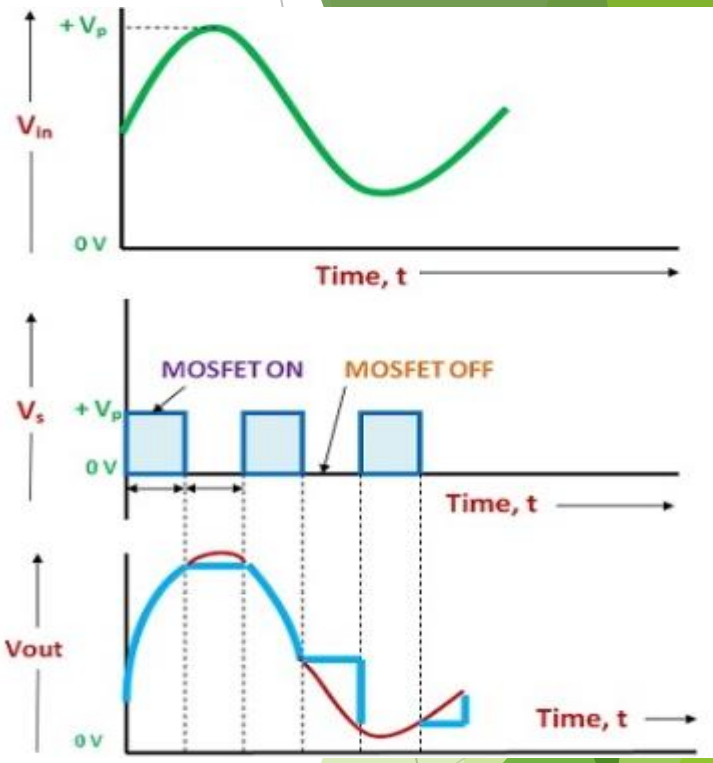
working

- Assume counter is reset to 0000,Ramp o/p is reset to 0V and analog i/p voltage is positive and i/p to the ramp generator/integrator is switched to the unknown analog i/p voltage.
- When positive analog i/p voltage is connected to the inverting i/p of the integrator and integrator o/p is a negative ramp, so comparator o/p is positive and clk is passed thru AND gate.
- Counter is incremented.
- Negative ramp will proceed for a time period T1.At the end,the ramp voltage is given by Vs=$\frac{Vi}{R*C}$*T1 where RC is the time constant of ramp generator circuit.
- When the counter reaches the fixed count at time period T1,the count detector gives a signal to the control circuit which resets the counter to zero and switches the integrator i/p to a negative reference,-Vr
- The ramp generator begins at –Vs and increases upward until it reaches 0V.The counter gets incremented.When Vs reaches 0V the comparator o/p becomes 0 and the clk will not pass thru AND gate.
- Conversion cycle is completed the positive ramp voltage is given by Vs=$\frac{-Vr}{R*C}$*T2
- Since the ramp generator starts at 0V decreasing down to –Vs and then increasing upto 0V, $\frac{Vi}{R*C}$*T1 =$\frac{-Vr}{R*C}$*T2 ---→ -Vi=Vr*$\frac{T2}{T1}$
- Ie.Unknown i/p is proportional to T2

SAMPLE AND HOLD CIRCUIT

- Samples an input signal and holds on to its last sampled value until the input is sampled again
- Useful in digital interfacing and analog to digital and PCM systems





- N channel E-MOSFET works as switch and is controlled by control signal and Capacitor stores charges.
- Analog signal is applied to the drain of E-MOSFET and control signal is applied to the gate.When control is positive E-MOSFET turns ON and capacitor charges to the instantaneous values of analog i/p with a time constant [Ro+rds(on)]C.where Ro is the o/p resistance of the voltage follower Z1 and rds(on) is the resistance of the MOSFET when ON

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- Thus the i/p appears across the capacitor and then at the o/p thru voltage follower Z2
- When control signal is zero,E-MOSFET is OFF.
- Capacitor is at high i/p impedance of the voltage follower Z2 and cannot discharge.It holds the voltage across it.
- Time during which voltage across the capacitor =i/p voltage➔sample period
- Time period during which the voltage across the capacitor is held constant ➔hold period
- Frequency of the control signal >2*i/p frequency inorder to retrieve the i/p from o/p waveform

Problems:

Eg 2.Basic step of a 9 bit DAC is 10.3mV.What o/p is produced if the i/p is 101101111?

Ans:Vo=10.3mV($1*2^8 + 0 * 2^7$+1*2^6+1*2^5+0*2^4+1*2^3+1*2^2+1*2^1+1*2^0)=10.3mV*367=3.78V

Eg 3.Calculate the values of LSB,MSB and full scale o/p for an 8 bit DAC for the 0 to 10 V range.

Ans:LSB=$\frac{10}{2^8}$=39mV

MSB=(1/2)*full scale voltage(FSV)=5V

Full scale o/p=FSV-1LSB=10-.039=9.961V

Eg 4.An 8 bit converter has an o/p of voltage range of 0 to 2.55V.Find resolution of the system and dynamic range.

Ans:Step size:$\frac{2.55}{2^8-1} = \frac{2.55}{255} = 10mV$ Dynamic range=$\frac{2.55}{10mV} = 255$ =48.13dB

Eg 5.What o/p voltage would be produced by a DAC whose o/p range is 0 to 10 V and input binary number is 10(for 2 bit)

Ans:Vo=10V($1*\frac{1}{2}$+$0*\frac{1}{4}$) $= 5V$

Eg 6.A 4 bit R-2R ladder type DAC have resistor values R=10K,2R=20K uses Vr of 10V.Find (a)resolution of DAC and(b)Io for a digital input of 1101.

Ans:(a)Resolution of 1 LSB=$\frac{1}{2^n} * \frac{Vr}{R}$=62.5μA.(b)Io= 62.5μA*13=0.8125mA

- 1.Let us find the value of analog output voltage of R-2R Ladder DAC for a binary input, b2b1b0=001
- 2.An 8 bit DAC has a resolution of 10mV/bit. Find the analog output voltage for the inputs(a)10001010(b)00010000
- 3.Calculate the values of LSB,MSB and full scale o/p for an 12 bit DAC for the 0 to 15 V range
- 4.What o/p voltage would be produced by a DAC whose o/p range is 0 to 12 V and input binary number is (a)11(for 2 bit) (b)1001(for 4 bit) (c) 10111111 (for 8 bit)
- 5.A system uses a 12 bit word to represent the input signal .Find the resolution and dynamic range.Given peak to peak voltage is set to 4V.
- 6.A 3 bit R-2R ladder type DAC have resistor values R=10K,2R=20K uses Vr of 10V.Find (a)resolution of DAC and(b)Io for a digital input of 100
- 7.Form a successive approximation sequence for number 210.
- 8.An 8 bit successive approximation ADC is driven by a 2MHz clock signal.Find the conversion time required.