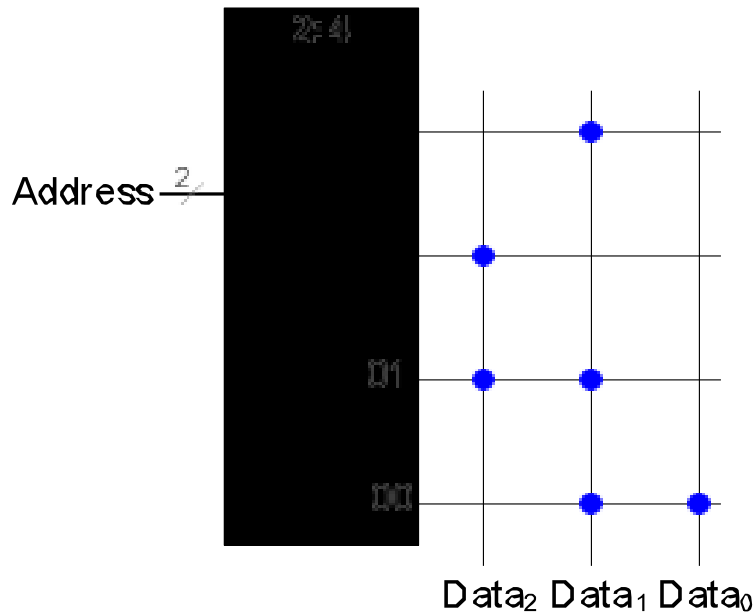# Memory Arrays

Digital Design and Computer Architecture

David Money Harris and Sarah L. Harris

ELSEVIER

ROM Storage

Address —2/—

2 : 4	
	01
	00

Data$_2$ Data$_1$ Data$_0$

Address	Data		
11	0	1	0
10	1	0	0
01	1	1	0
00	0	1	1

depth

width

$$Data_2 = \underline{A_1} \oplus A_0$$

$$Data_1 = \underline{A_1} + \underline{A_0}$$
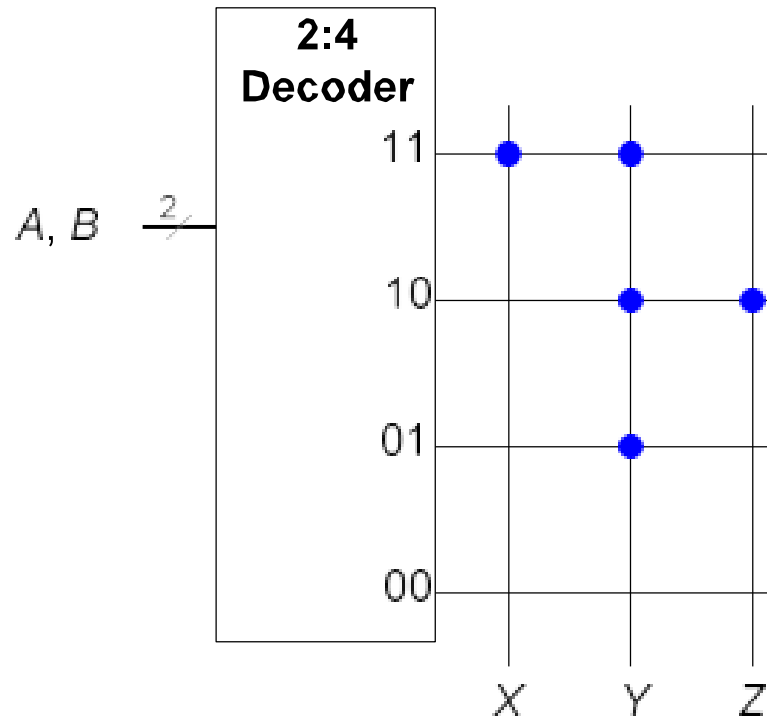
$$Data_0 = A_1 A_0$$

Example: Logic with ROMs

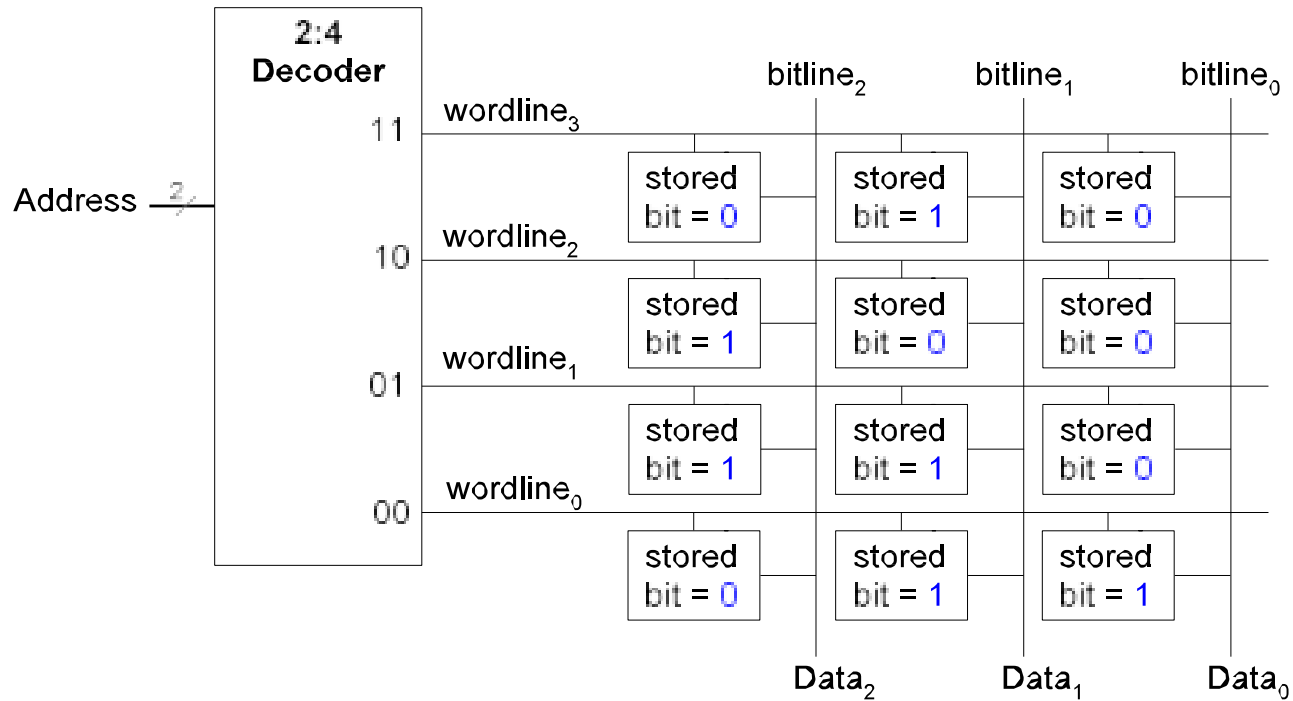- Implement the following logic functions using a $2^2 \times 3$-bit ROM:
  - $X = AB$
  - $Y = A + B$
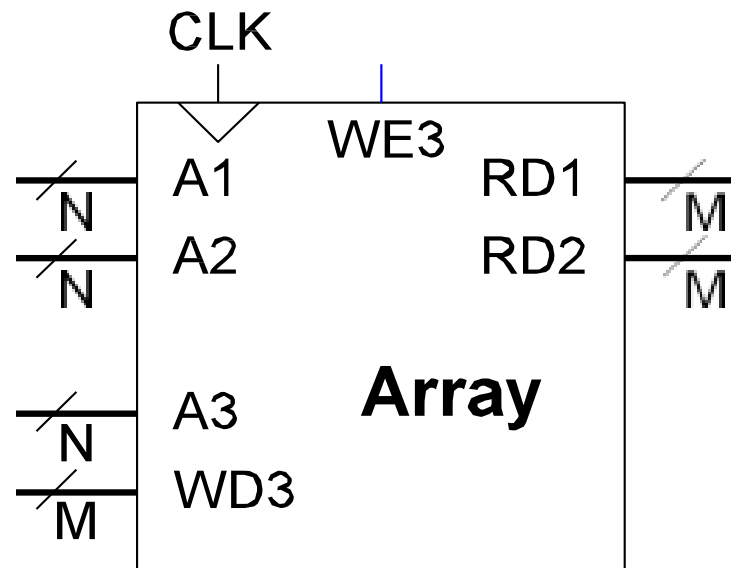 - $Z = A\,\overline{B}$

Logic with Any Memory Array

$$Data_2 = A_1 \oplus A_0$$

$$Data_1 = \overline{A_1} + A_0$$

$$Data_0 = \overline{A_1}\,\overline{A_0}$$

Multi-ported Memories

- **Port:** address/data pair
- 3-ported memory
  - 2 read ports (A1/RD1, A2/RD2)
  - 1 write port (A3/WD3, WE3 enables writing)
- Small multi-ported memories are called *register files*

```
          CLK
           │
           ▼        WE3
    ──/──┤ A1          RD1 ├──/──
      N  │              RD2 │   M
    ──/──┤ A2               ├──/──
      N  │                  │   M
         │
    ──/──┤ A3      Array
      N  │
    ──/──┤ WD3
      M  │
```
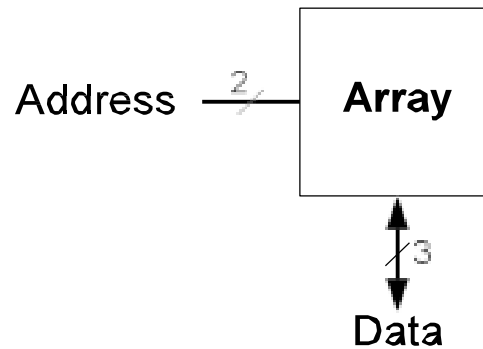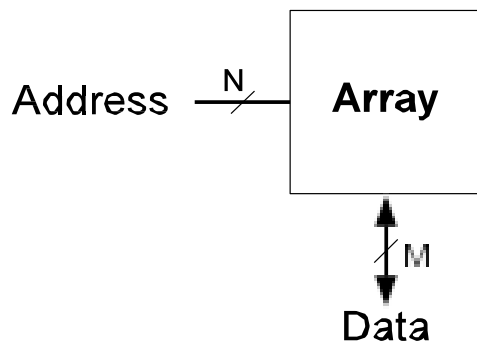
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Memory Arrays

- Efficiently store large amounts of data
- Three common types:
  - Dynamic random access memory (DRAM)
  - Static random access memory (SRAM)
  - Read only memory (ROM)
- An M-bit data value can be read or written at each unique N-bit address.

Address $\xrightarrow{\quad N \quad}$ **Array** $\updownarrow M$ Data
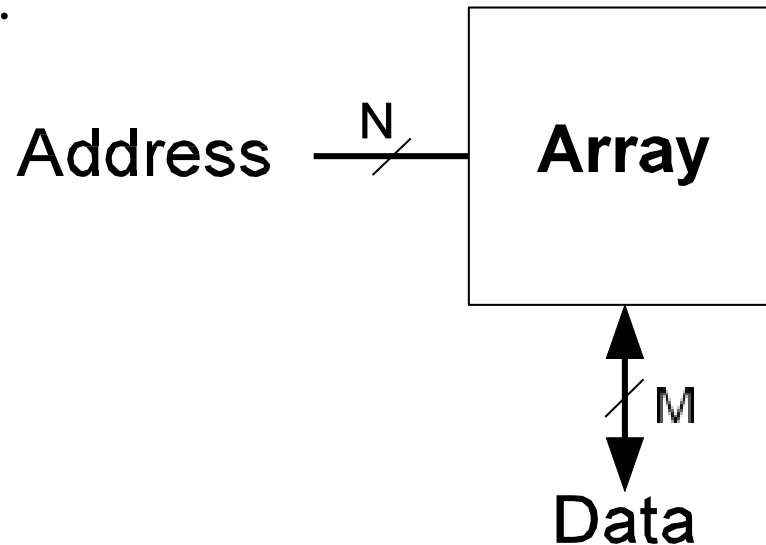
Memory Arrays

- Two-dimensional array of bit cells

- Each bit cell stores one bit

- An array with N address bits and M data bits:
  - 2^N rows and M columns
  - **Depth:** number of rows (number of words)
  - **Width:** number of columns (size of word)
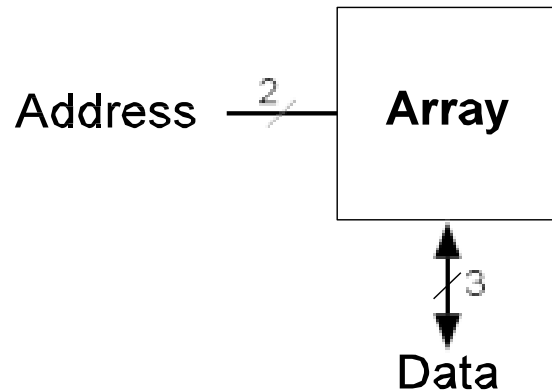 - **Array size:** depth × width = $2^N \times M$

Memory Array: Example

- $2^2 \times$ 3-bit array

- Number of words: 4

- Word size: 3-bits

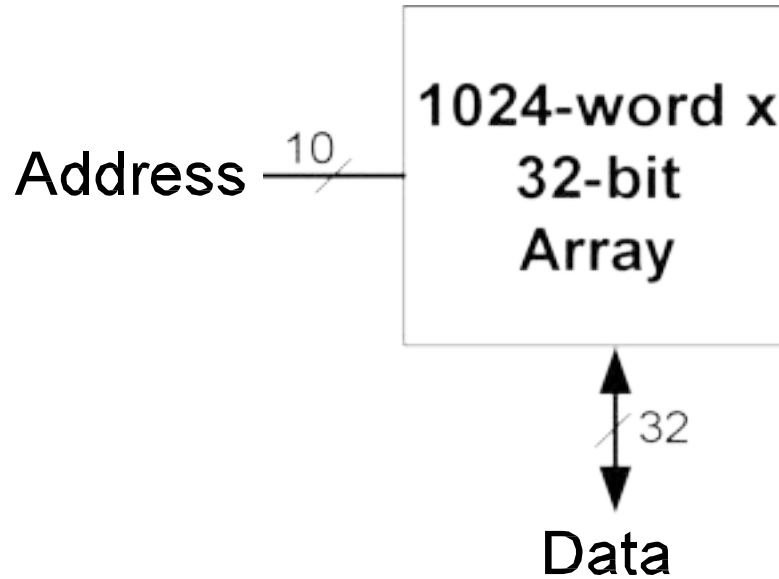- For example, the 3-bit word stored at address 10 is 100
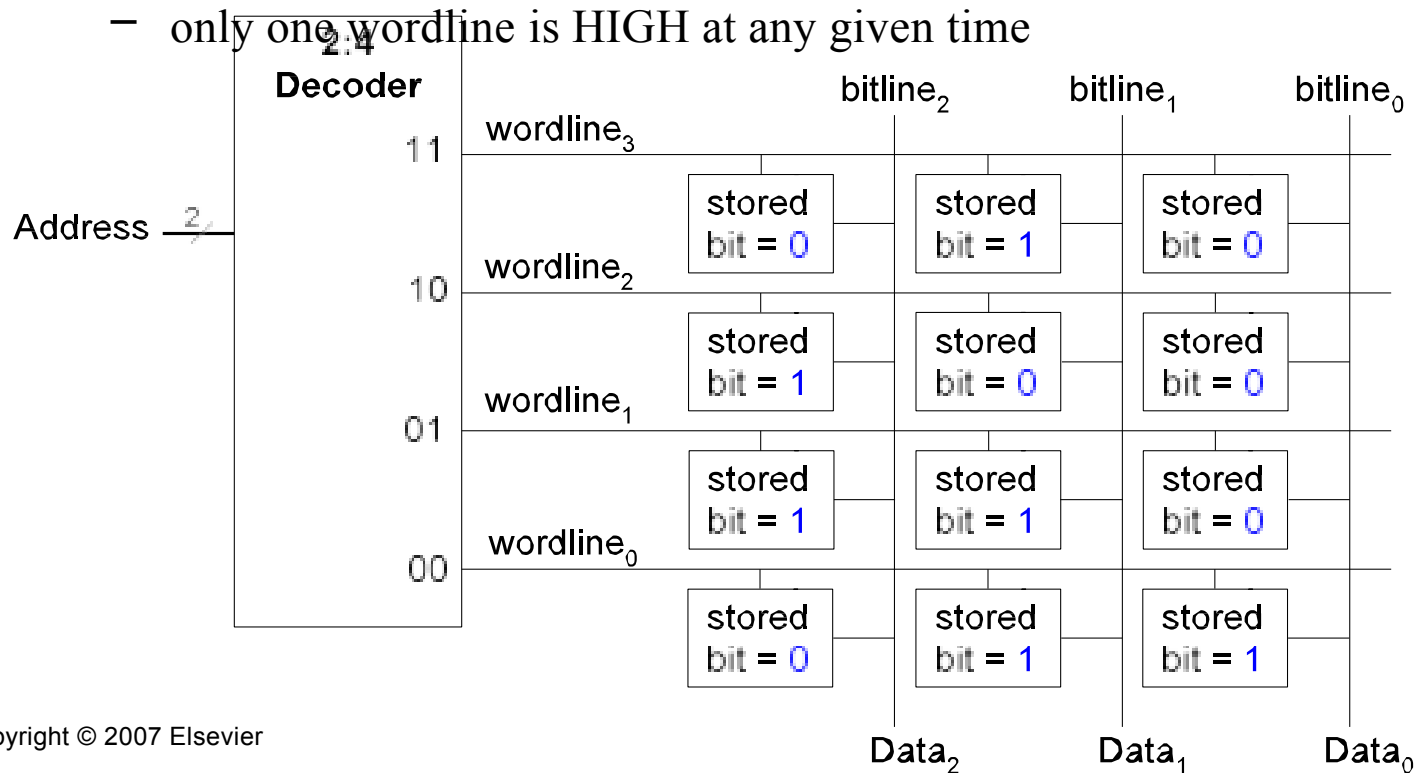
Example:

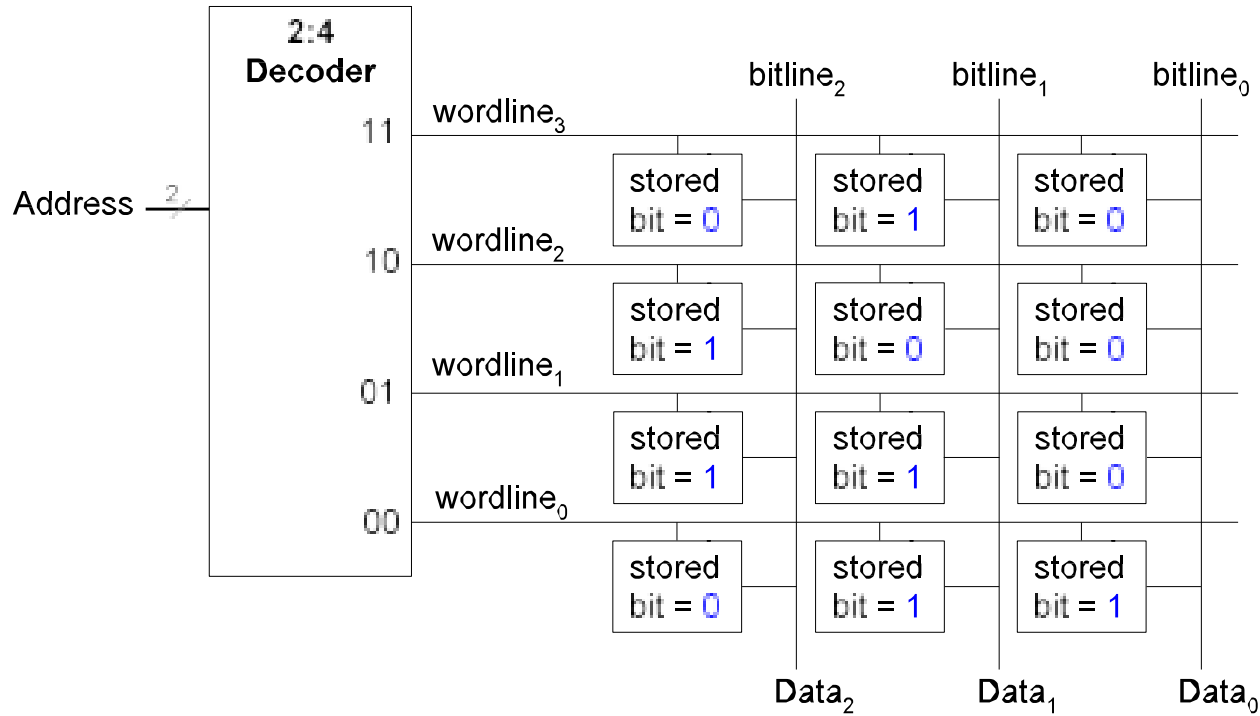ELSEVIER

Memory Arrays
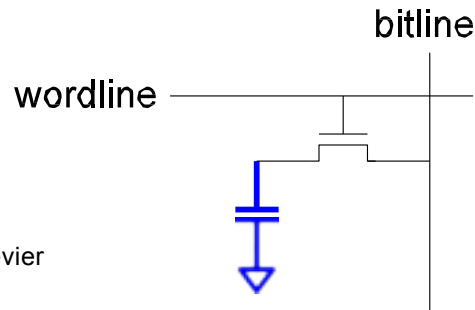
Memory Array

- **Wordline:**
  - similar to an enable
  - allows a single row in the memory array to be read or written
  - corresponds to a unique address
  - only one wordline is HIGH at any given time

Memory Arrays

DRAM bit cell:

SRAM bit cell: