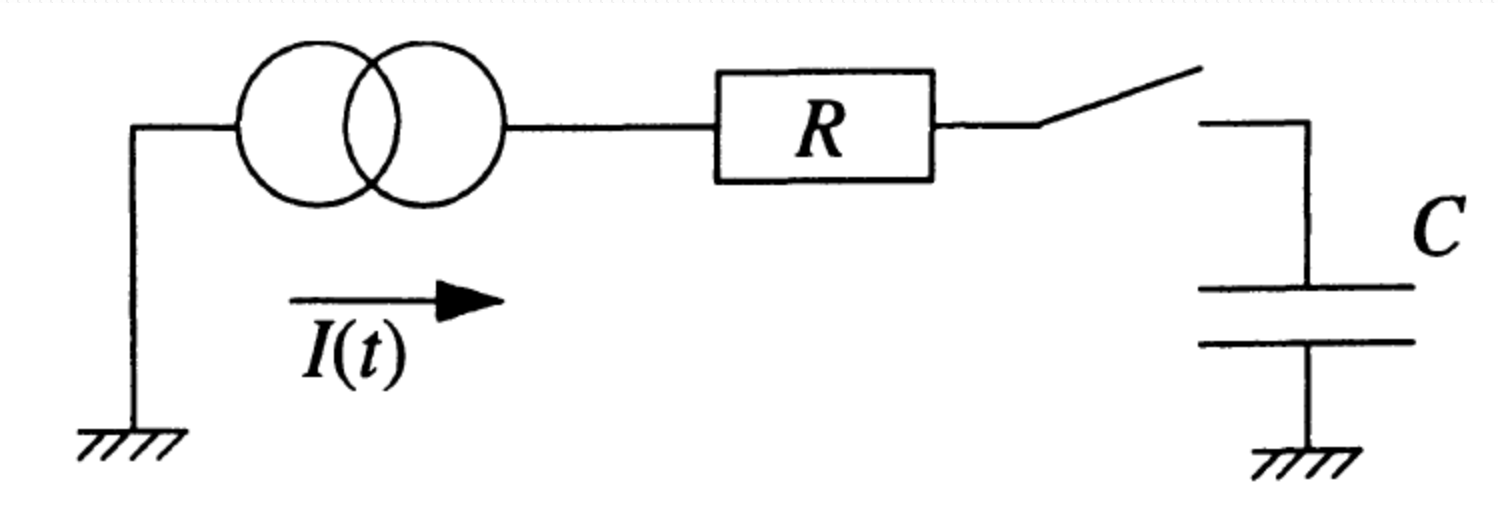
EC 464 – LPVLSI

Module VI

Adiabatic Charging

- I(t) – time-dependent current source



- The capacitance voltage as a function of time, $V_C(t)$, is then given by:

$$V_C(t) = \frac{1}{C}\int_0^t I(\theta)d\theta = \frac{1}{C}\tilde{I}(t)t$$

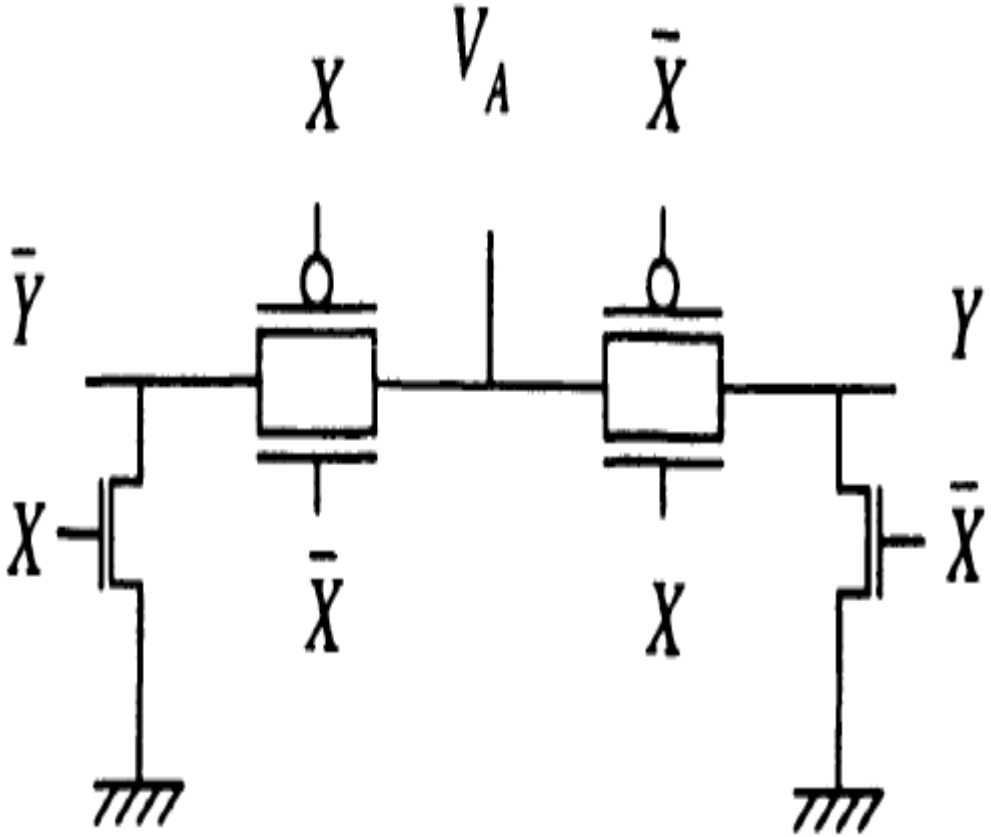
$\tilde{I}(t)$ is the average current from 0 to t:

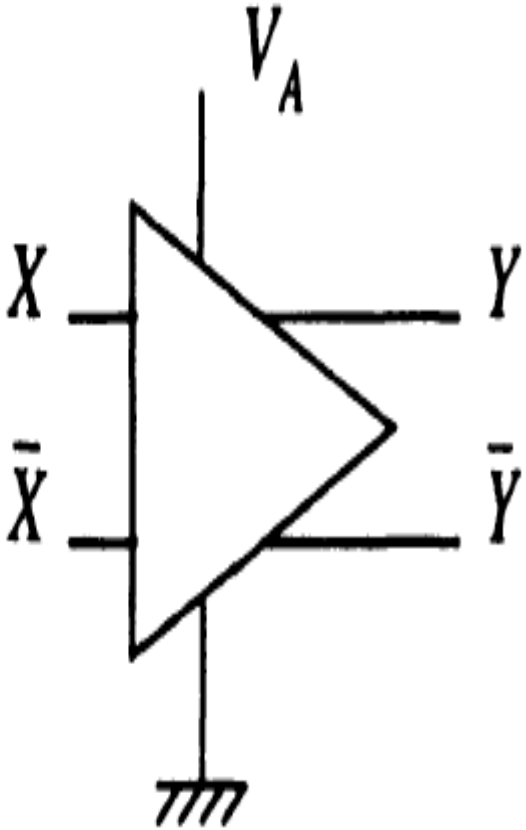
$$\tilde{I}(t) = \frac{C \cdot V_C(t)}{t}$$

The energy dissipation in R from 0 to $t = T$ is then given by:

$$E_{\text{diss}} = R\int_0^T I(\theta)^2 d\theta \geq R\int_0^T \tilde{I}(T)^2 d\theta = R\tilde{I}(T)^2 T = \frac{RC}{T}CV_C(T)^2$$

Adiabatic Amplification





It consists of two transmission gates (T-gates) and two NMOS clamps.
The input and output are dual-rail encoded

Operation

- input is set to a valid value: X and X`
- Amplifier is "energized" by applying to VA a slow voltage ramp from 0 to V_{dd}
- One of the outputs is adiabatically charged to Vdd while the other is clamped to ground
- When charging is complete, the output signal pair is valid
- The amplifier is de-energized by ramping the voltage on V_A back to 0.

- Both devices are in the triode region, conductance of the NMOS device, G_n

$$G_n = \frac{C_n}{K_n}(V_{dd} - V_{ch} - V_{th})$$

$$K_n = \frac{L^2}{\mu_n}$$

Vch – average channel voltage,
Vth –threshold voltage,
Cn – gate capacitance of the device.
Kn – process constant
L– channel length,
μ_n – mobility

conductance of the PMOS device

$$G_p = \frac{C_p}{K_p}(V_{ch} - V_{th})$$

One-Stage Adiabatic Buffer

- Ein – input Energy
- α – a proportionality constant

$$\alpha = (C_n + C_p)/C_n$$

- The dissipation caused by driving the inputs of one of the T-gates is given by:

$$E_{in} = \alpha C_n V_{dd}^2$$

- The total energy dissipated per cycle for one driven output is

$$E_{total} = E_{in} + E_{load} = \alpha C_n V_{dd}^2 + \left(2\xi \frac{\tau_n}{T} \frac{1}{(m-2)} \frac{C_L}{C_n}\right) C_L V_{dd}^2$$

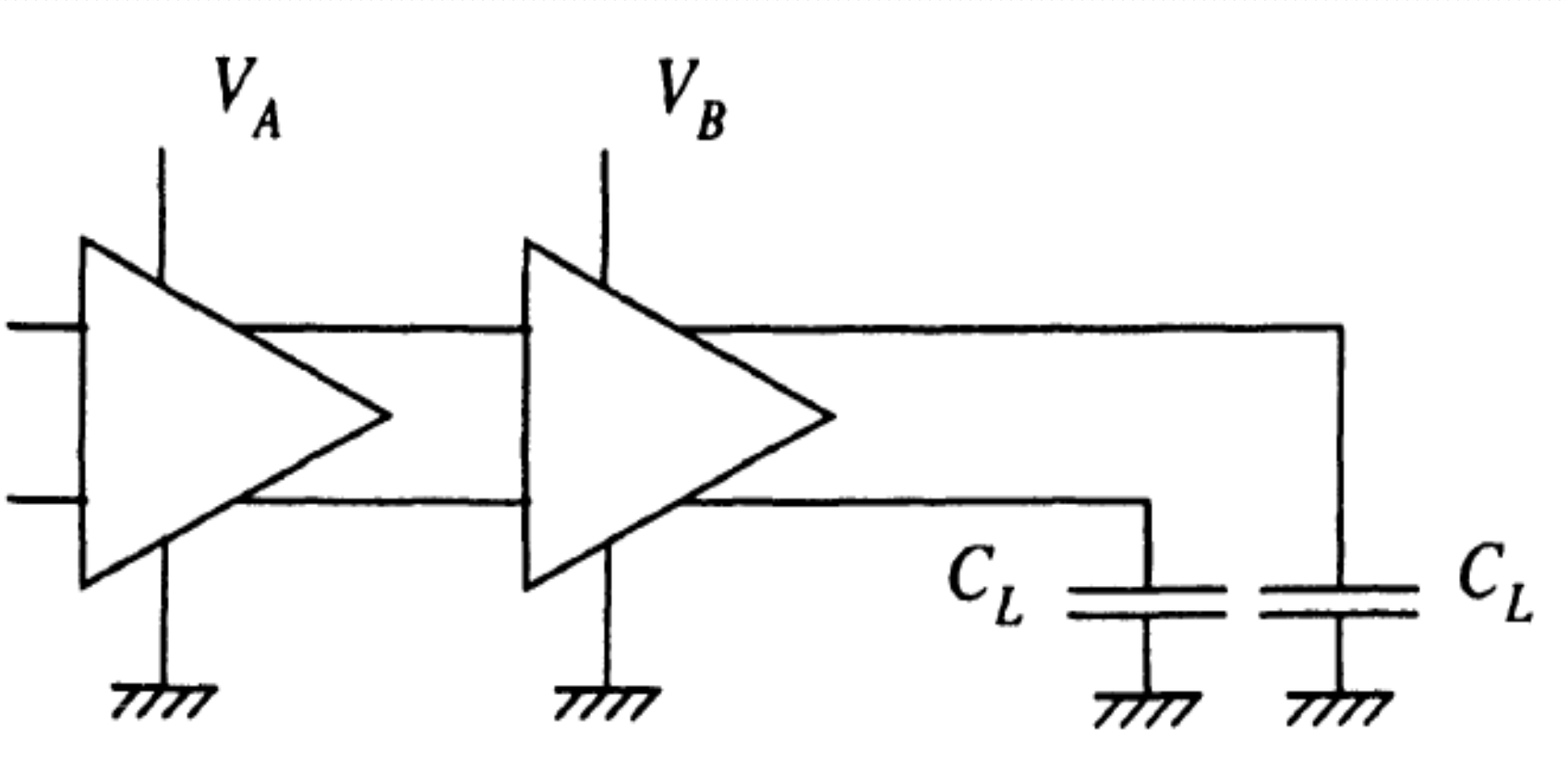
- The optimum NMOS gate capacitance is

$$C_{n_{opt}} = \sqrt{\frac{2\xi}{\alpha}\frac{\tau_n}{T}\frac{1}{(m-2)}}C_L$$

- Minimum dissipation is

$$E_{total_{min}} = \sqrt{8\xi\alpha\frac{\tau_n}{T}\frac{1}{(m-2)}}C_L V_{dd}^2 = \sqrt{8\xi\alpha\frac{\tau_n}{T}\frac{m^4}{(m-2)}}C_L V_{th}^2$$

Two-Stage Adiabatic Buffer



Fully-Adiabatic System

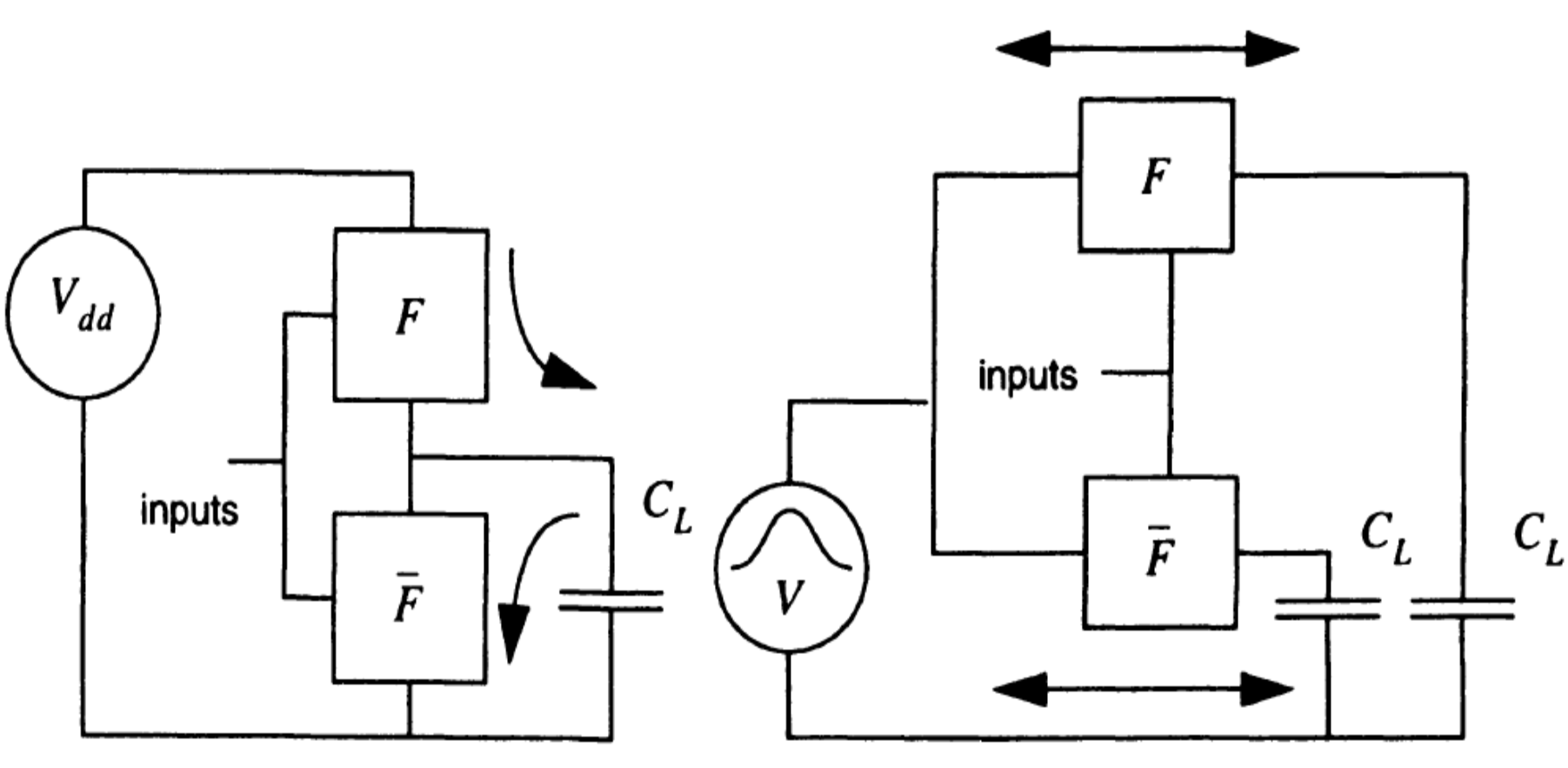
- The dissipation for driving the load and the inputs of the second amplifier is

$$E_{total_{min}} = \left(2\xi\frac{\tau_n}{T}\frac{1}{(m-2)}\right)\left(\frac{\alpha^2 C_{n2}^2}{C_{n1}} + \frac{C_L^2}{C_{n2}}\right)V_{dd}^2$$

$$C_{n2_{opt}} = \sqrt[3]{\frac{C_L^2 C_{n1}}{2}}$$

$$E_{total} = \left(2\xi\frac{\tau_n}{T}\frac{1}{(m-2)}\left(\sqrt[3]{2} + \frac{1}{\sqrt[3]{4}}\right)\sqrt[3]{\frac{C_L}{C_{n1}}}\right)C_L V_{dd}^2$$

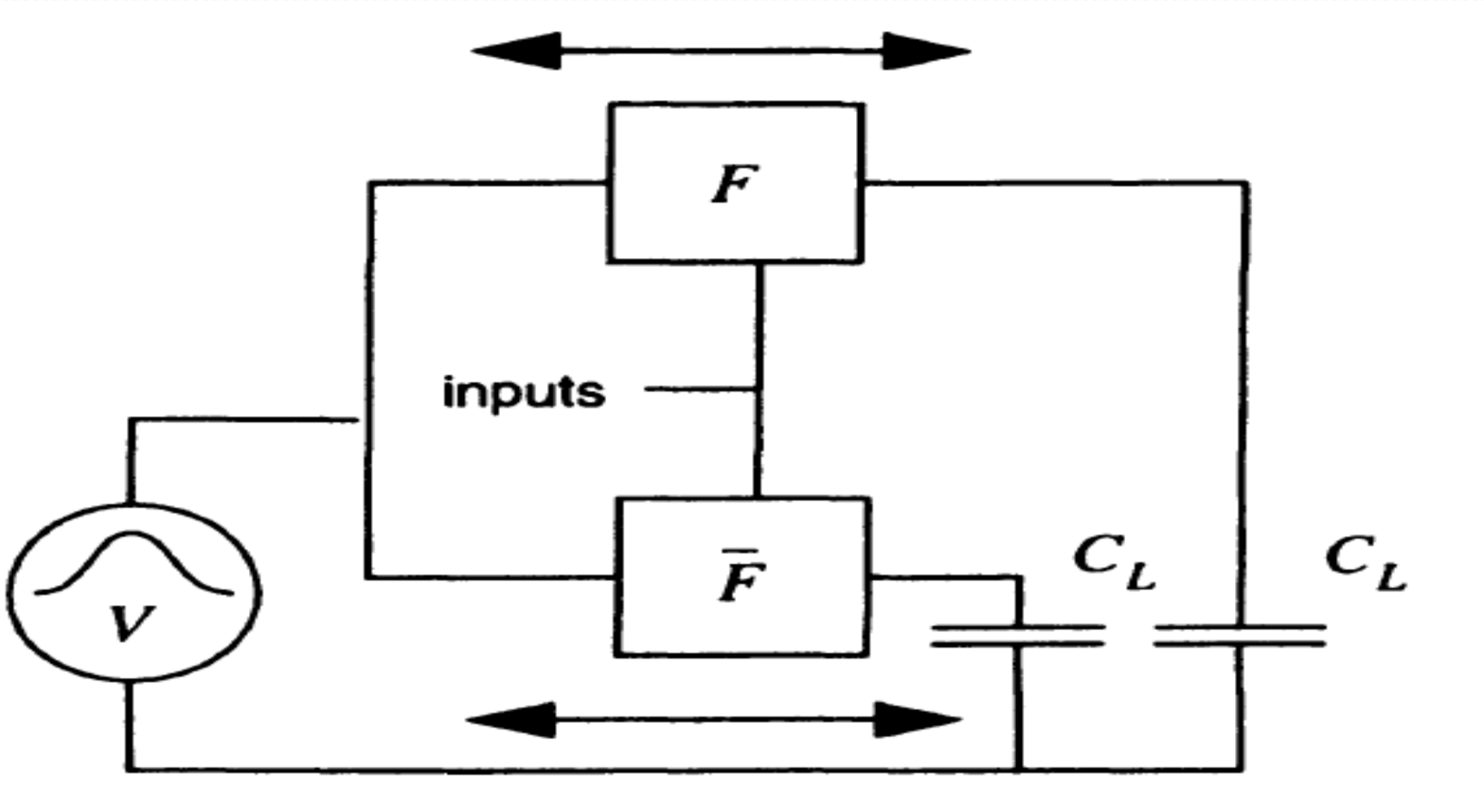
Adiabatic Logic Gates



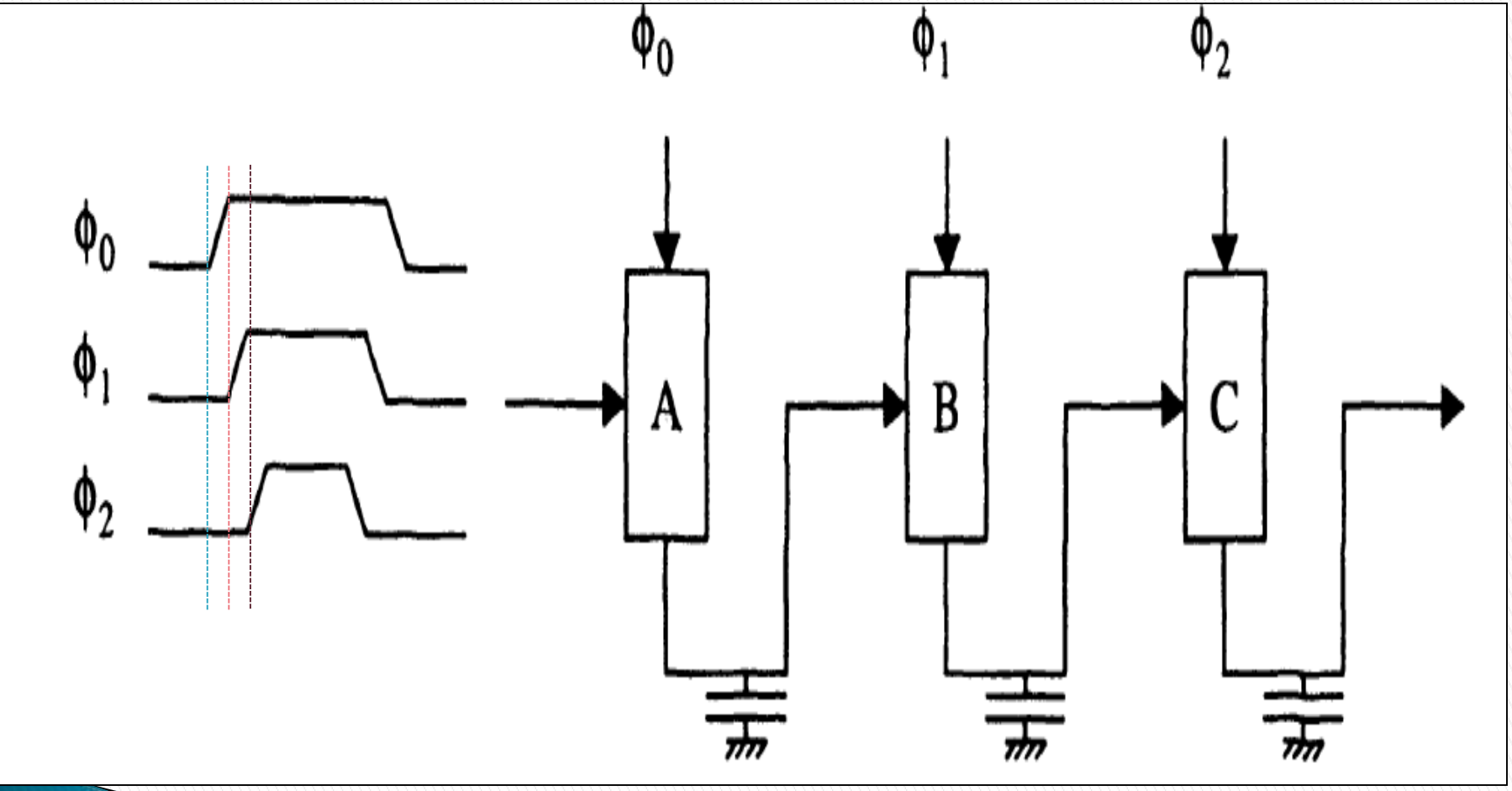
Conventional CMOS Logic

Adiabatic CMOS Logic

Adiabatic Logic Gates



Retractile cascade of adiabatic-switching logic gates



Retractile cascade

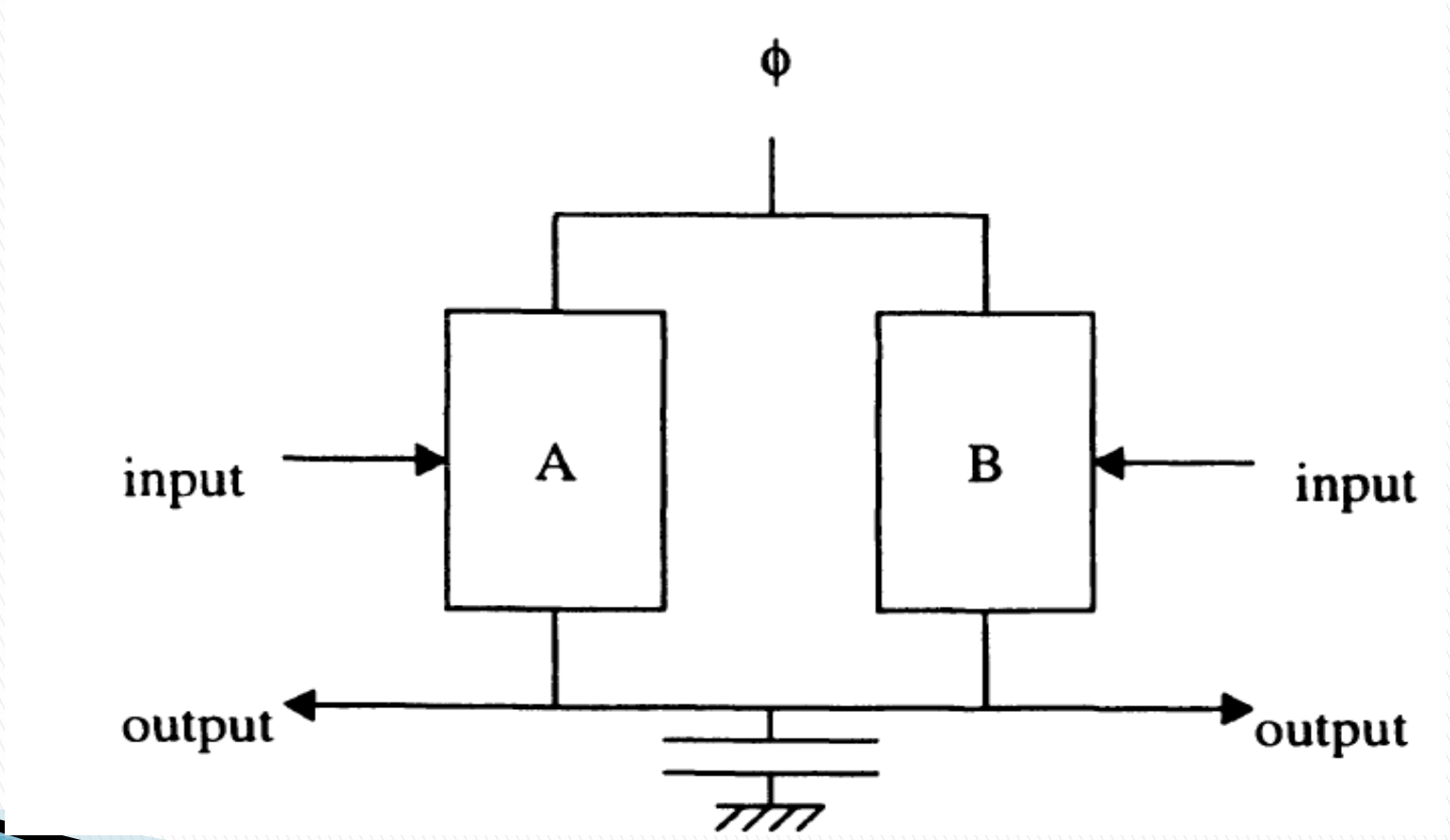
- Adiabatic operation is possible only if the inputs of every gate are held stable while the gate is energized
- The gates must then be de-energized in reverse order before the input values to the cascade may change

Disadvantage

- They require a large and possibly indeterminate number of supply voltage waveforms
- Waveforms have different pulse widths

Pipelinable adiabatic gate

- Pipelining can be used to improve the throughput of the system



Simple inductive power supply