MODULE 1-ANALOG INTEGRATED CIRCUITS

CREDITS-4

COURSE CODE: EC 204

Syllabus

Differential amplifier configurations, Operational amplifiers, Block diagram, Ideal op-amp parameters, Effect of finite open loop gain, bandwidth and slew rate on circuit performance, op-amp applications-linear and nonlinear, Active filters, Specialized ICs and their applications, Monolithic Voltage Regulators - types and its applications, Data converters - specifications and types.

Expected outcome .

The students will

i. have a thorough understanding of operational amplifiers
ii. be able to design circuits using operational amplifiers for various applications

Text Books:

1. Franco S., Design with Operational Amplifiers and Analog Integrated Circuits, 3/e, Tata McGraw Hill, 2008
2. Salivahanan S. ,V. S. K. Bhaaskaran, Linear Integrated Circuits, Tata McGraw Hill, 2008

References:

1. Botkar K. R., Integrated Circuits, 10/e, Khanna Publishers, 2010
2. C.G. Clayton, Operational Amplifiers, Butterworth & Company Publ. Ltd. Elsevier, 1971
3. David A. Bell, Operational Amplifiers & Linear ICs, Oxford University Press, 2^{nd} edition, 2010
4. Gayakwad R. A., Op-Amps and Linear Integrated Circuits, Prentice Hall, 4/e, 2010
5. R.F. Coughlin & Fredrick Driscoll, Operational Amplifiers & Linear Integrated Circuits, 6^{th} Edition, PHI,2001
6. Roy D. C. and S. B. Jain, Linear Integrated Circuits, New Age International, 3/e, 2010
7. Sedra A. S. and K. C. Smith, Microelectronic Circuits, 6/e, Oxford University Press, 2013

Course Plan

Module	Contents	Hours	Sem. Exam Marks
I	Differential amplifiers: Differential amplifier configurations using BJT, Large and small signal operations, Input resistance, Voltage gain, CMRR, Non-ideal characteristics of differential amplifier. Frequency response of differential amplifiers, Current sources, Active load, Concept of current mirror circuits, Wilson current mirror circuits (Analysis using hybrid 'pi' model only).	6	15%
	Operational amplifiers: Introduction, Block diagram, Ideal op-amp parameters, Equivalent circuit, Voltage transfer curve, Open loop op-amp configurations, Effect of finite open loop gain, Bandwidth and slew rate on circuit performance	5	
II	Op-amp with negative feedback: Introduction, Feedback configurations, Voltage series feedback, Voltage shunt feedback, Properties of practical op-amp.	3	15%
	Op-amp applications: Inverting and non inverting amplifier, DC and AC amplifiers, Summing, Scaling and averaging amplifiers, Instrumentation amplifier.	4	
	FIRST INTERNAL EXAMINATION		
III	Op-amp applications: Voltage to current converter, Current to voltage converter, Integrator, Differentiator, Precision rectifiers, Log and antilog amplifier, Phase shift and Wien bridge oscillators	7	15%
IV	Astable and monostable multivibrators, Triangular and saw tooth wave generators, Comparators, Zero crossing detector, Schmitt trigger	5	15%
	Active filters: Advantages, First and second order low pass, High pass, Band pass and band reject filters, Design of filters using Butterworth approximations	5	
	SECOND INTERNAL EXAMINATION		
V	Specialized ICs and its applications: Timer IC 555 : Astable and monostable operations, applications. Analog Multipliers: Introduction, Gilbert multiplier cell. Voltage Controlled Oscillator IC AD633 and their applications.	3	20%
	Phase Locked Loop – Operation, Closed loop analysis, Lock and capture range, Basic building blocks, PLL IC 565, Applications of PLL for AM & FM detection and Frequency multiplication, Frequency division, Frequency synthesizing.	4	
	Monolithic Voltage Regulators - Fixed voltage regulators, 78XX and 79XX series, Adjustable voltage regulators, IC 723 – Low voltage and high voltage configurations, Current boosting, Current limiting, Short circuit and Fold-back protection.	4	
VI	Data Converters: D/A converter, Specifications, Weighted resistor type, R-2R Ladder type.	3	20%
	A/D Converters: Specifications, Classification, Flash type, Counter ramp type, Successive approximation type, Single slope type, Dual slope type, Sample-and-hold circuits.	5	
	END SEMESTER EXAM		

DIFFERENTIAL AMPLIFIERS USING BJT

- Positive input –Vce1 will be less positive.ie.inverting o/p
- Ie1 increases which increases the voltage drop across Re
- Both emitter sides will be positive,whichis eqwt to a

Negative base of T2

- Thus Vce2 increases and a noninverting o/p is obtained.
- This is based on the i/p signal at base of T1.
- DIFFERENTIAL MODE INPUT and OUTPUT

Vid=Vi1-Vi2

- i/p is applied to both inputs(same magnitude but

opposite polarity) and o/p obtained as the difference

between two o/ps

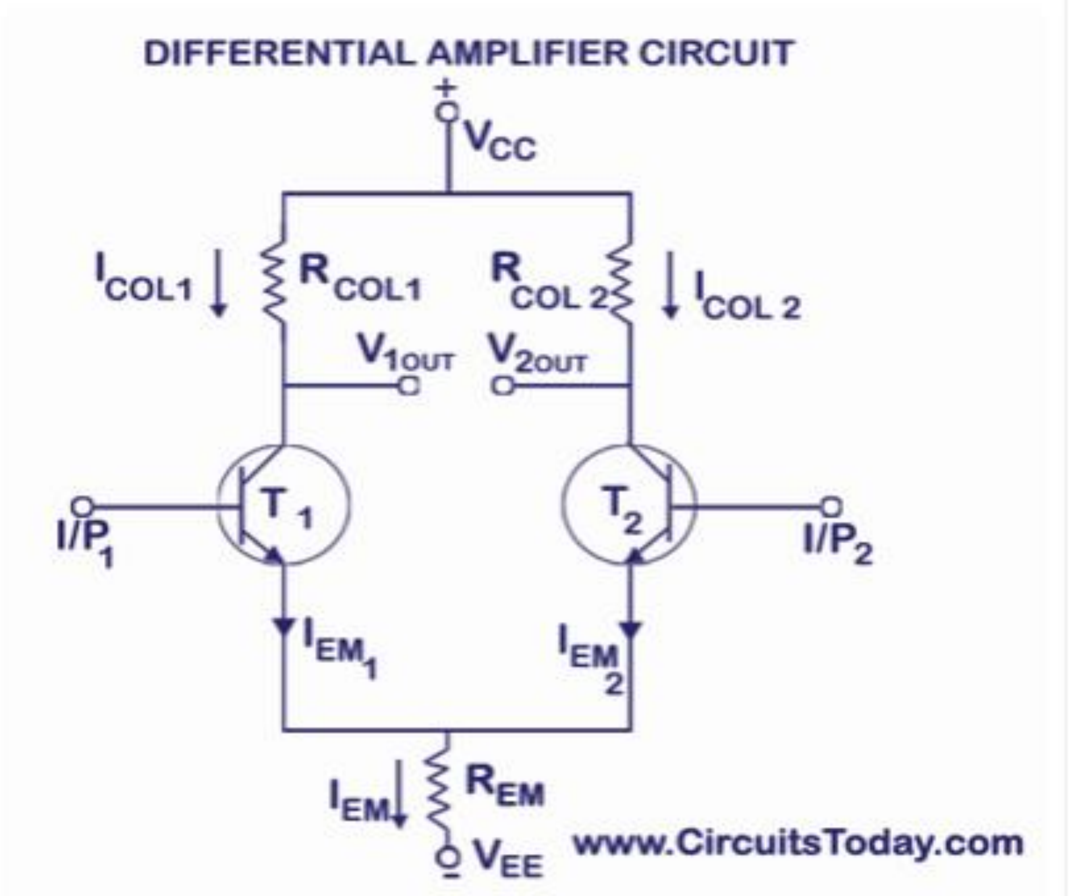
Vod=Vo1-Vo2

- DIFFERENTIAL MODE GAIN

Ad=Vod/Vid

- COMMON MODE INPUT and OUTPUT-i/p is made common to both(same magnitude and same phase)

$Vic=\frac{Vi1+Vi2}{2}$;Voc is of same phase



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- DIFFERENTIAL MODE GAIN:Ad=$\frac{\text{Vod}}{Vid}$
- COMMON MODE GAIN:Ac=$\frac{Voc}{Vic}$
- COMMON MODE REJECTION RATIO,CMRR=$\frac{Ad}{Ac}$=δ
- Usually CMRR=∞
- Total o/p=Vo=Vod+Voc=AdVid+AcVic

=AdVid(1+$\frac{AcVic}{AdVid}$)= AdVid(1+$\frac{Vic}{\delta Vid}$)≈AdVid for δ>>1

- PROPERTIES AND ADVANTAGES:

Excellent stability ,High versatility, High immunity to noise, lower cost, easier fabrication as IC and closely matched components.

According to the way the i/p signals are applied and o/p signal is taken,different configurations are as follows:

- Dual input balanced output (o/p measured between two collectors)
- Dual input unbalanced output
- Single input balanced output
- Single input unbalanced output

DIFFERNTIAL MODE GAIN

- Input is applied between two bases.When Vi1 increases

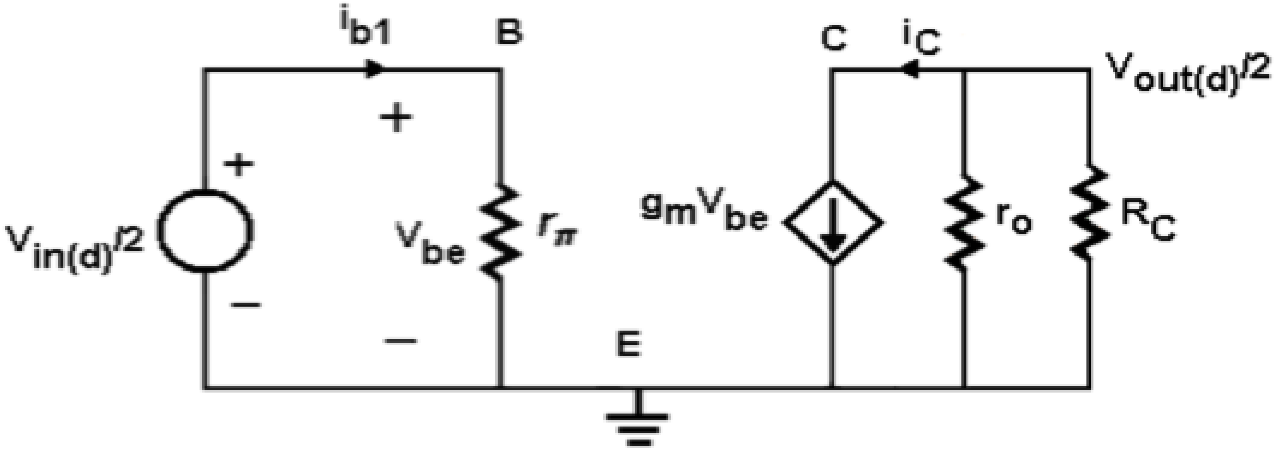
Vi2 decreases,ic1 increases and ic2 decreases.

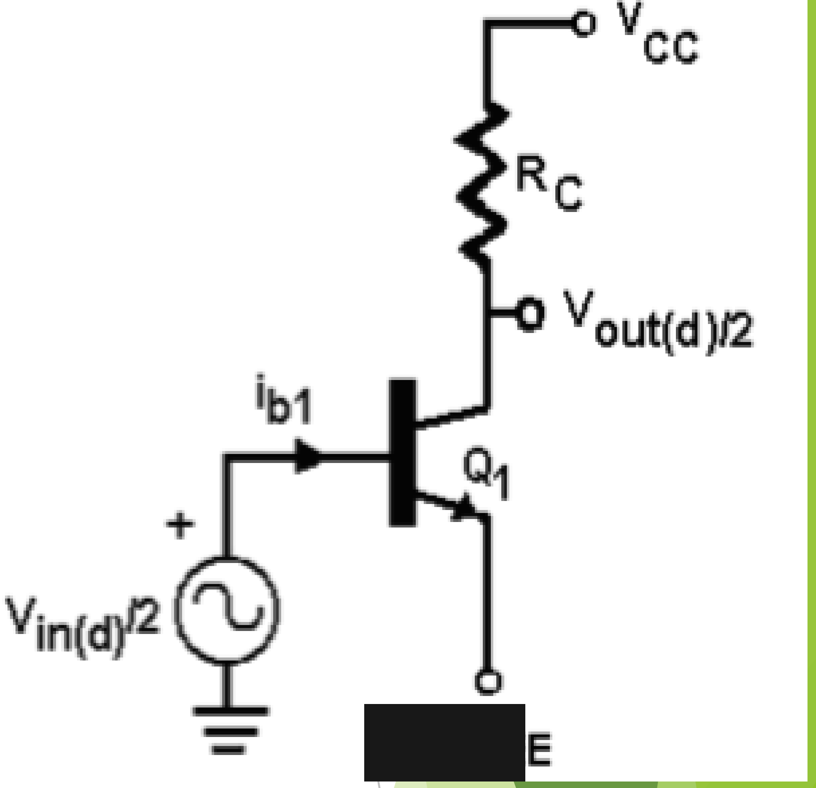
ie1=ic1+ic2 remains constant and can be considered at ground potential

Hence RE has no significance in ac operations

Based on the analysis, the ac differential input circuit of the amplifier

can be splitted into two half circuits-eqwt circuit is drawn:





$\frac{Vout}{2}$=-gm$\frac{Vin}{2}$(Rc||ro)

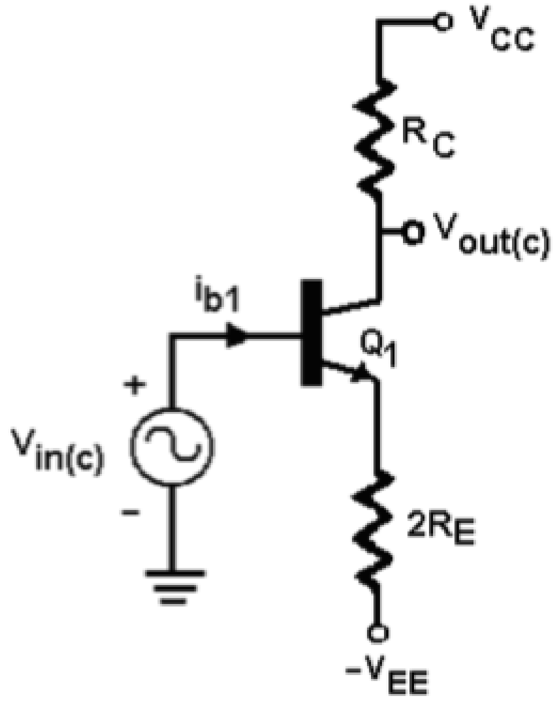
$\frac{Vo}{Vin}$=-gm(Rc||ro);**Ad=-gmRc**Vin/2=ib1*r∏ **Rid=2*r∏ =2(1+β)re**

Vod/2=ic(Rc||ro); **Rod=2(Rc||ro)**

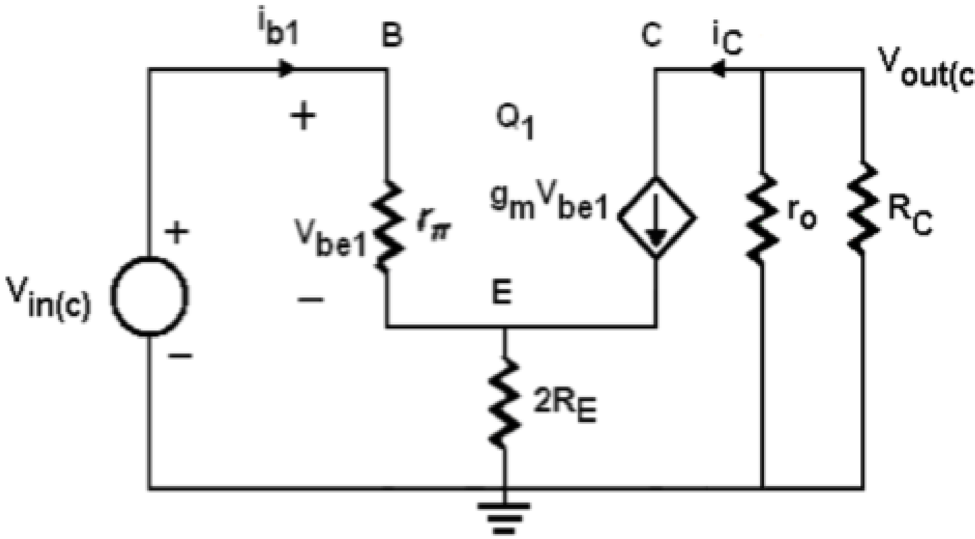
If o/p is taken at one collector,Ad=$\frac{-gmRc}{2}$ rπ=(1+β)re

COMMON MODE GAIN

Since emitter voltage at emitter E1 and E2 is changing, therefore, the emitter resistance of the half circuit should be 2RE instead of RE after splitting into two half circuits



- Vin(c) = ib1rπ +ib1(β+1)2RE(by resistance reflection rule)
- Common-mode input resistance **Rin(c) = [rπ + (β +1)2RE]**
- common-mode output resistance **Rout(c) is equal to (RC||ro).**
- Vout(c) = -icRc,Vin(c) =ie*2RE≈ic*2RE
- Ac=Vout/Vin=-Rc/2RE
- **CMRR=Ad/Ac=$\frac{-gmRc}{-Rc/2RE}$=2gmRE**



CMRR can be increased by

- Increasing gm:

gm=Ic/0.025.increase Ic.requires larger power supply

But Ri=βRE =β(0.025/Ic) thus Ri decreases

- Increasing RE:

Requires larger power supply(eg:ic=1mA,If Re=1MΩ,Vbe=10^6*1/10^3=1000V

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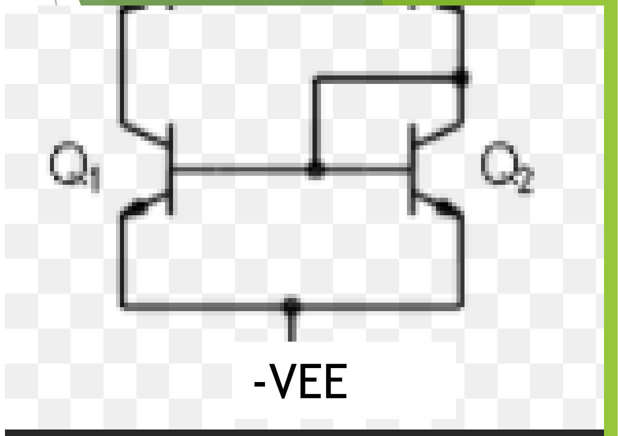
- Re can be used without increasing power supply replacing active resistance with constant current source



Problems:

(1)Rc1=Rc2=2.2K,Re=4.7K,Vin1=50mV,Vin2=20mV,Vee=-10V,Vcc=10V.Find Ic1,Vce1 Ad,Ac,CMRR,Vo

Soln:Vcc=IcRc+IeRe;Ie=$\frac{Vcc-IcRc}{Re}$ =10-0.7/4.7K=1.97mA

Ic1=Ic2=1.97/2=0.99mA

Vc1=Vcc-Ic1*Rc1=10-0.99mA*2.2K=7.8V

Vce1=Vc1-Ve1=7.8-0.7=7.1V

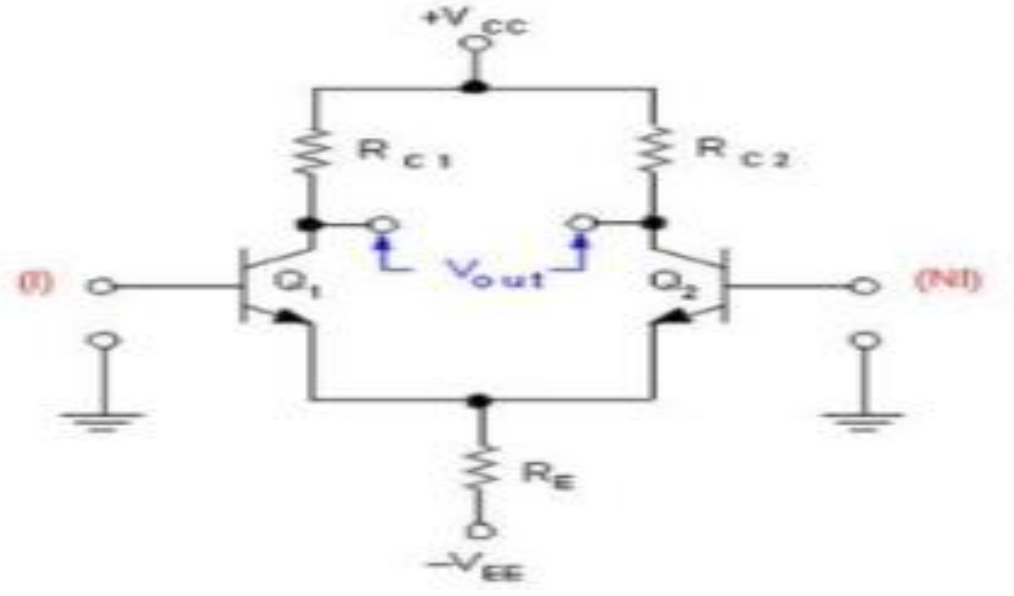
Gm=Ic/.025=40mA/V   Ad=-gmRc=-40mA*2.2K=-88

Ac=-Rc/2Re=-2.2K/2*4.7K=-0.23

CMRR=2gmRc=2*40m*4.7K=376

Vid=Vin1-Vin2;Vic=(Vin1+Vin2)/2

Vo=AdVid+AcVic=88*30mV+0.23*35mV=2.64+0.0085=2.6485



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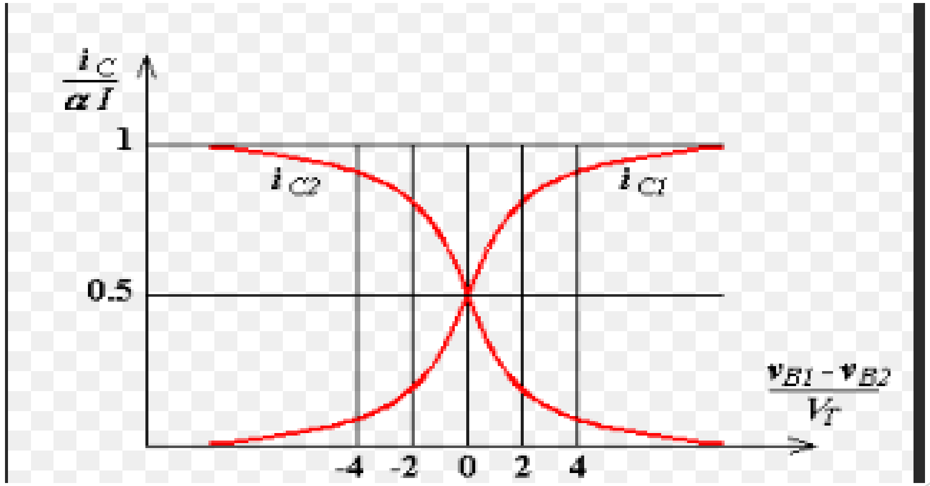
- Rid=2*β*re=2*100*0.025/Ic=5K
- Vc=Vcc-IcRc,Vce=Vc-Ve=Vcc-IcRc+Vbe=([10-1*2.2K]/1000)+0.7=8.5V

- Problem 2:CMRR=1000,Vi1=100μV, Vi1=-100μV,Find Vo
- Vid=Vi1-Vi2=200μV,Vic=(Vi1+Vi2)/2=0V
- **Vo=AdVid[1+Vic/∂Vid]**
- Ad*200μV[1+0]=200μVAd

- Problem 3:Vi1=1100μV,Vi2=900μV,Vid=200μV,Vic=1000μV,Find Vo

LARGE SIGNAL OPERATION

- $Ie1=Io*e^{\frac{(Vb1-Ve)}{VT}}$ $Ie2=Io*e^{\frac{(Vb2-Ve)}{VT}}$ $\frac{Ie1}{Ie2}=e^{\frac{(Vb1-Vb2)}{VT}}$
- $1+\frac{Ie1}{Ie2}=1+e^{\frac{(Vb1-Vb2)}{VT}}$ $\frac{Ie1+Ie2}{Ie2}=1+e^{\frac{(Vb1-Vb2)}{VT}}$ $\frac{Ie2}{Ie1+Ie2}=\frac{1}{1+e^{\frac{(Vb1-Vb2)}{VT}}}$
- $Ie2=\frac{I}{1+e^{\frac{(Vb1-Vb2)}{VT}}}$ Similarly $Ie1=\frac{I}{1+e^{\frac{(Vb2-Vb1)}{VT}}}$
- $Ic=\alpha Ie$
- Variation of normalized collector current ic/I versus difference In base voltage(Vb1-Vb2)/Vt is illustrated by transfer characteristics
- If Vb1=Vb2 the total current I divides equally between the two transistors.
- If considered as small signal amplifier, difference input signal is limited to a very low value.Transistors operate in the linear segment around A



NON IDEAL CHARCTERISTICS OF DIFFERENTIAL AMPLIFIER

- Amplify the difference component ,Reject the noise component
- Ideal characteristics of Differential Amplifier:

1. Infinite differential Gain
2. Infinite input resistance
3. Zero output resistance
4. Infinite CMRR
5. Infinite Bandwidth
6. Zero o/p voltage for zero difference i/p signal

Due to the mismatches in load resistors,deviates from its ideal chara:

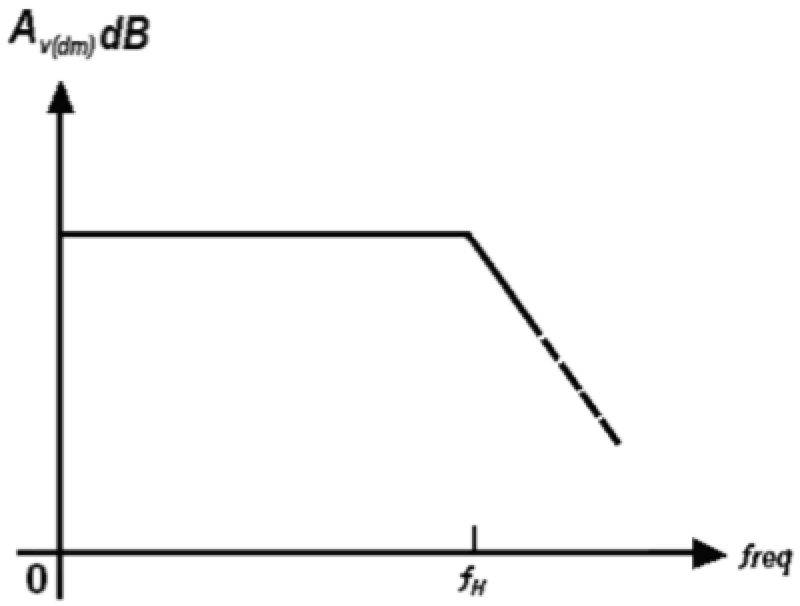
1. Input offset voltage
2. Input offset current
3. Input common mode range

FREQUENCY RESPONSE OF DIFFERENTIAL AMPLIFIER

- If the base resistor RB is added to the bipolar junction transistor differential amplifier circuit, then the differential mode voltage gain
- AV(dm) shall be Av(dm) = $-gmRc\frac{r\Pi}{r\Pi+Rb}$
- From the earlier analysis of high frequency response of the common-emitter configuration, the differential mode voltage gain transfer function is Av(dm)(s) = $-gmRc\frac{r\Pi}{r\Pi+Rb}$ $*\frac{1}{1+s(r\Pi||Rb(C\Pi+Cm)}*\frac{1}{1+sRc(C\mu+Cce)}$
- Cm-Millers capacitance =Cμ(1+gmRc) where Cμ=collector to base capacitance
- Two critical frequencies,fH=$\frac{1}{2\Pi[r\Pi||Rb(C\Pi+Cm)]}$ fH1=$\frac{1}{2\Pi[Rc(C\mu+Cce)]}$
- As Cce,Cμ and Rc is small,frequencies are infinite
- Since there is no coupling capacitor in the circuit,

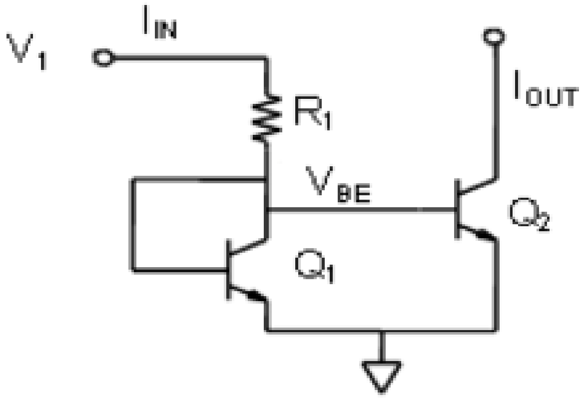
the bandwidth different mode gain shall be from 0 Hz frequency

to fH.



CONSTANT CURRENT SOURCE

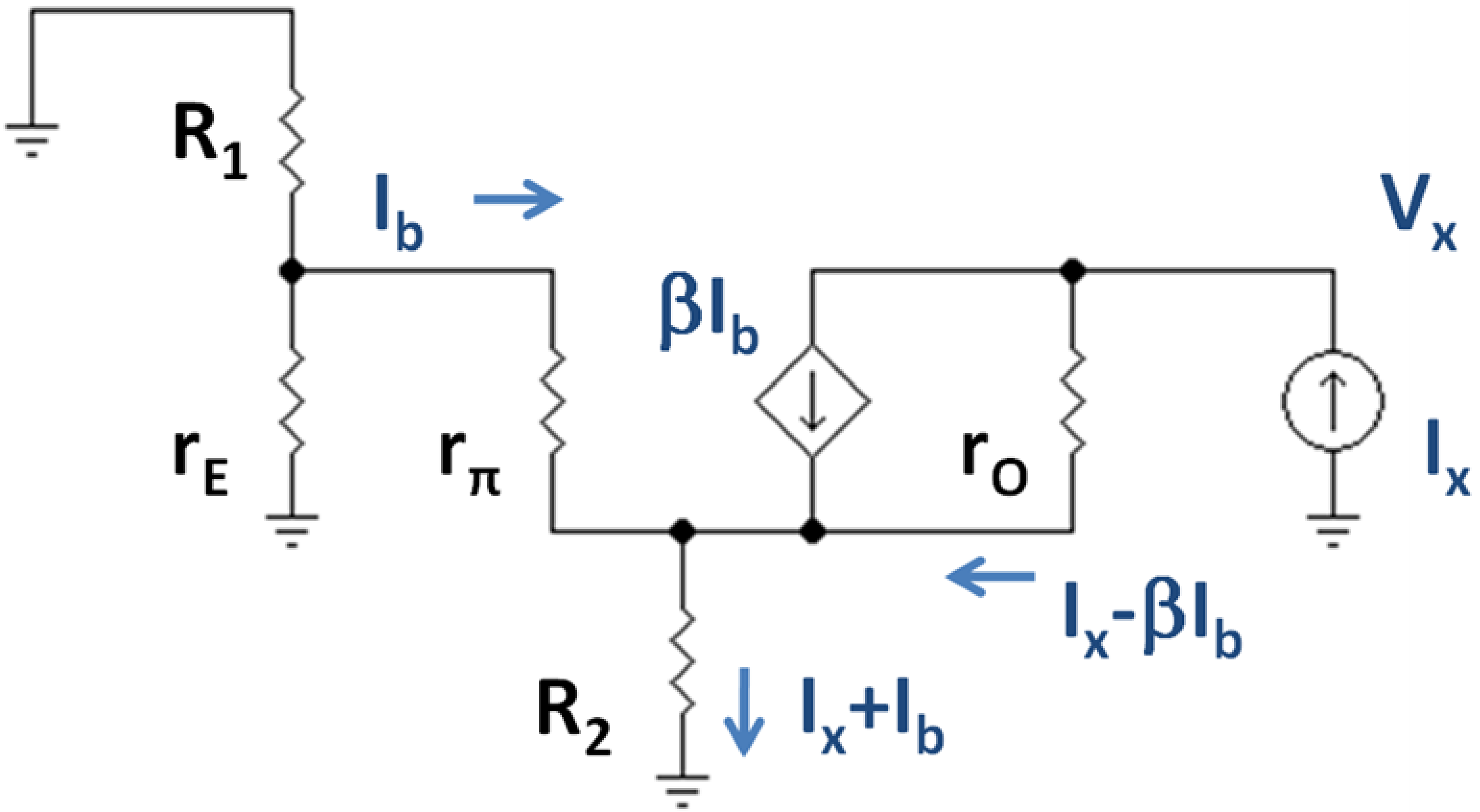
- CMRR to be large Acm->0 as Re->∞ then Vee should be increased to maintain the quiescent current
- If operating currents are decreased this decreases CMRR
- Solution: of Re

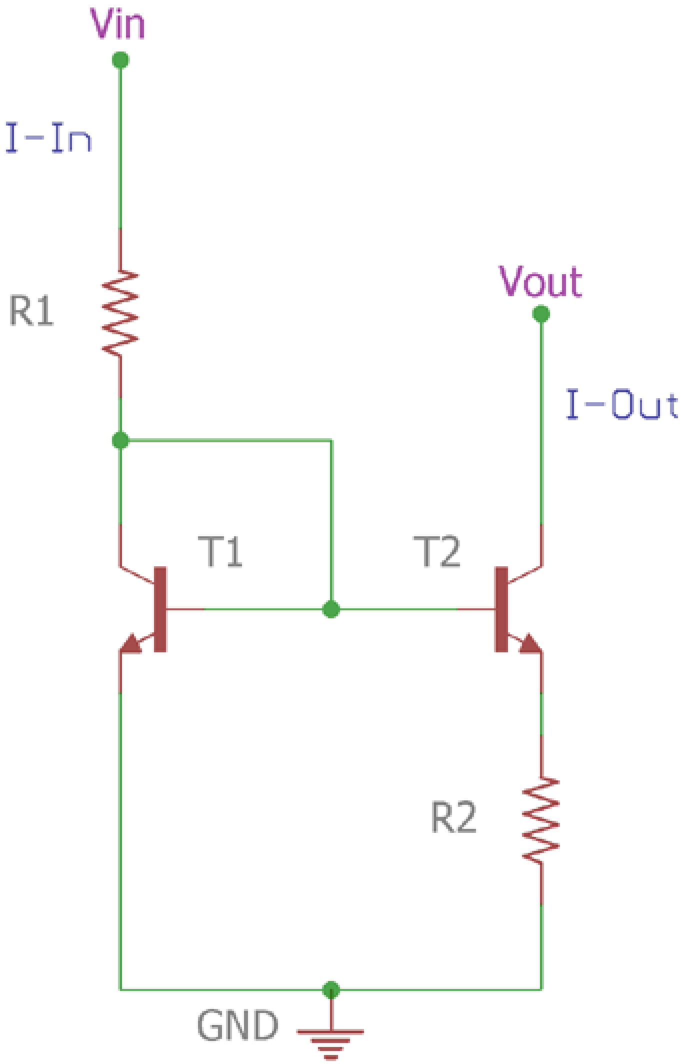


- Q1 and Q2 matched,same Vbe.Q1 is shorted to collector from base.Voltage is established across Q2.emitter currrents will be same.Collector currents equal to Iref.output current is a **REFLECTION OR MIRROR** of the reference current.Circuit is referred to as a current mirror.

WIDLAR CURRENT SOURCE

- Need low value current source - R1 is high in basic current mirror circuit.
- Due to R2,Vbe2 <Vbe1 and Iout<Iin





Analysis

- Output resistance is found using a small-signal model
- Transistor Q_1 is replaced by its small-signal emitter resistance r_E because it is diode connected. Transistor Q_2 is replaced with its hybrid-pi model. A test current I_x is attached at the output.

$$I_b\left[(R_1 \parallel r_E) + r_\pi\right] + [I_x + I_b]R_2 = 0\ .$$

$$I_b = -I_x \frac{R_2}{(R_1 \parallel r_E) + r_\pi + R_2}\ .$$

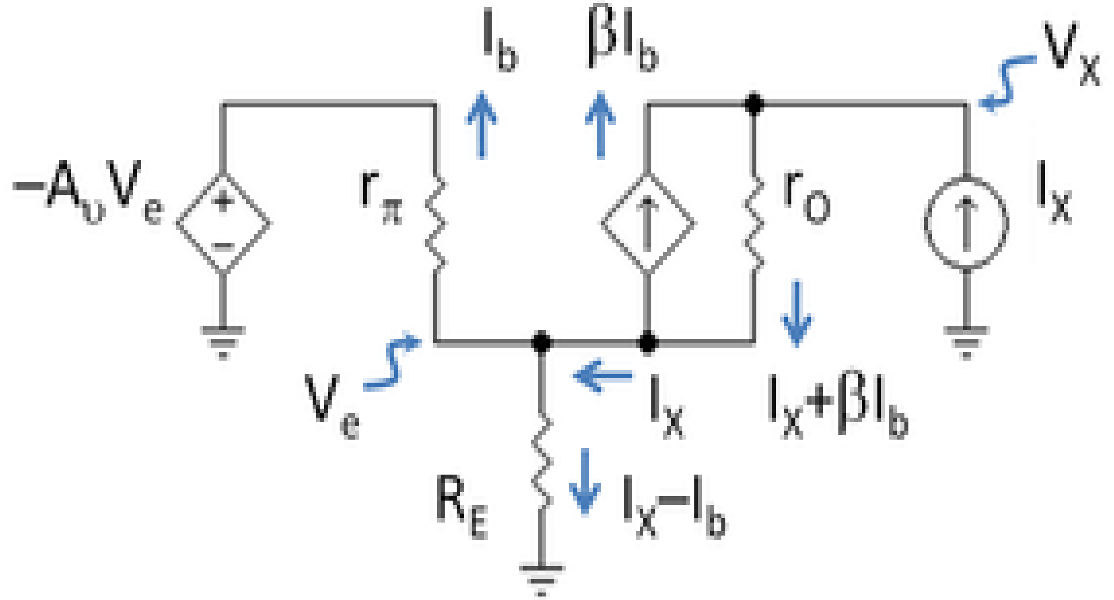
$$V_x = I_x(R_2 + r_O) + I_b(R_2 - \beta r_O)\ ,$$

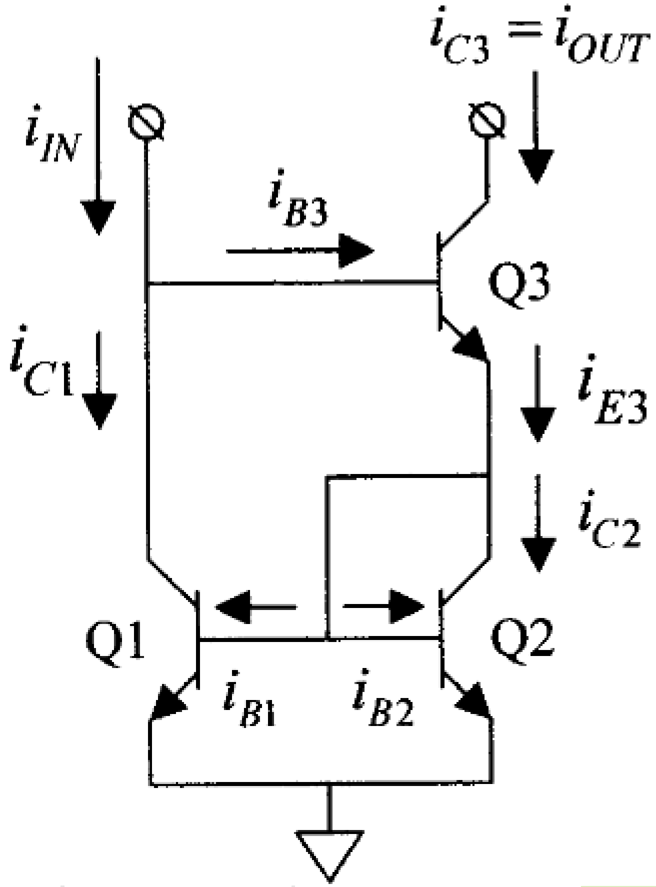
- Substituting for Ib

$$R_O = \frac{V_x}{I_x} = r_O\left[1 + \frac{\beta R_2}{(R_1 \parallel r_E) + r_\pi + R_2}\right] + R_2\left[\frac{(R_1 \parallel r_E) + r_\pi}{(R_1 \parallel r_E) + r_\pi + R_2}\right]\ .$$

- the output resistance of the Widlar current source is increased over that of the output transistor itself (which is r_O) so long as R_2 is large enough compared to the r_π of the output transistor.
- The output transistor carries a low current, making r_π large, and increase in R_2 tends to reduce this current further, causing a correlated increase in r_π. The resistance $R_1 \| r_E$ usually is small because the emitter resistance r_E usually is only a few ohms.

WILSON CURRENT MIRROR





$$I_b = \frac{V_e}{r_\pi/(A_v+1)} \,.$$

$$I_b = I_X \frac{R_E}{R_E + \frac{r_\pi}{A_v+1}} \,.$$

$$V_X = (I_X + \beta I_b) r_O + (I_X - I_b) R_E \,.$$

$$R_{out} = \frac{V_X}{I_X} = r_O \left(1 + \beta \frac{R_E}{R_E + r_\pi/(A_v+1)}\right) + R_E \| \frac{r_\pi}{A_v+1} \,.$$

$$R_{out} = (\beta + 1) r_O \,,$$

basic mirror where $R_{out} = r_O$

- To achieve higher resistance than ro of simple current source
- An additional transistor Q3 is connected as a negative feedback which increases the o/p resistance
- This cancels base currents and makes Io/Iin less sensitive to β
- Thus Io=Iin and Wilson current source offers a very high resistance

Since Vbe1=Vbe2,Ic1=Ic2,Ib1=Ib2=Ib

$I_{B3} = I_{C3} / \beta$ … (1)

$I_{E3} = I_{C3} + I_{B3}$

$I_{E3} = ((\beta + 1)/ \beta)\ I_{C3}$ … (2)

$I_{E3} = I_{C2} + I_{B1} + I_{B2}$

$I_{E3} = I_{C2} + I_{B} + I_{B}$

$I_{E3} = I_{C2} + 2I_{B}$

$I_{E3} = (1+(2/\beta))\ I_{C2}$------------(3)

$(1+(2/\beta))\ I_{C2} = ((\beta + 1)/ \beta)\ I_{C3}$

$$I_{C3} = Io = \frac{(\beta + 2)}{(\beta + 1)} I_{C1} \text{ AS } I_{C1} = I_{C2}$$

Iin=Ic1+Ib3

$$Iin = \frac{(\beta + 2)}{(\beta + 1)} I_{C1} + I_{B3}$$

$$Iin = \frac{(\beta + 2)}{(\beta + 1)} I_{C1} + Io/\beta$$

$$Io = \frac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2} Iin$$ where Iin=(Vcc-2Vbe)/R1

$$Io - Iin = \frac{2}{\beta^2 + 2\beta + 2} Iin$$

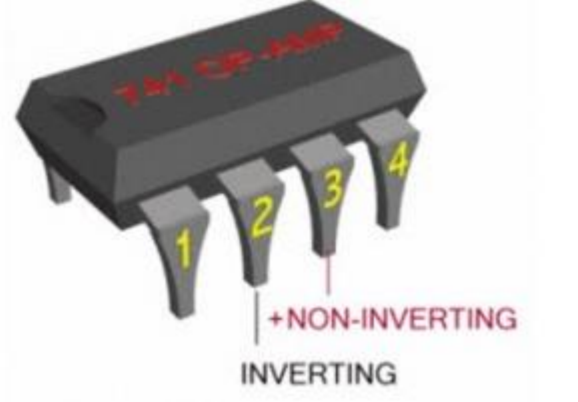
Output resistance is >>> β r0/2 than widlar current source

ADVANTAGES OF WILSON CURRENT MIRROR:

- In case of basic current mirror circuit, the base current mismatch is a common problem. However, this Wilson current mirror circuit virtually eliminates the base current balance error.
- Due to this, the output current is near to accurate as of the input current. Not only this, the circuit employs very high output impedance due to the negative feedback across the T1 from the base of the T3.
- The improved Wilson current mirror circuit is made using 4 transistor versions so it is useful for the operation at high currents.
- The Wilson current mirror circuit provides low impedance at the input.
- It doesn't require additional bias voltage and minimum resources are needed to construct it.
- **LIMITATIONS OF WILSON CURRENT MIRROR:**
- When the Wilson current mirror circuit is biased with maximum high frequency the negative feedback loop cause instability in frequency response.
- It has a higher compliance voltage compared with the basic two transistor current mirror circuit.
- Wilson current mirror circuit creates noise across the output. This is due to the feedback which raises output impedance and directly affect the collector current. The collector current fluctuation contributes noises across the output.

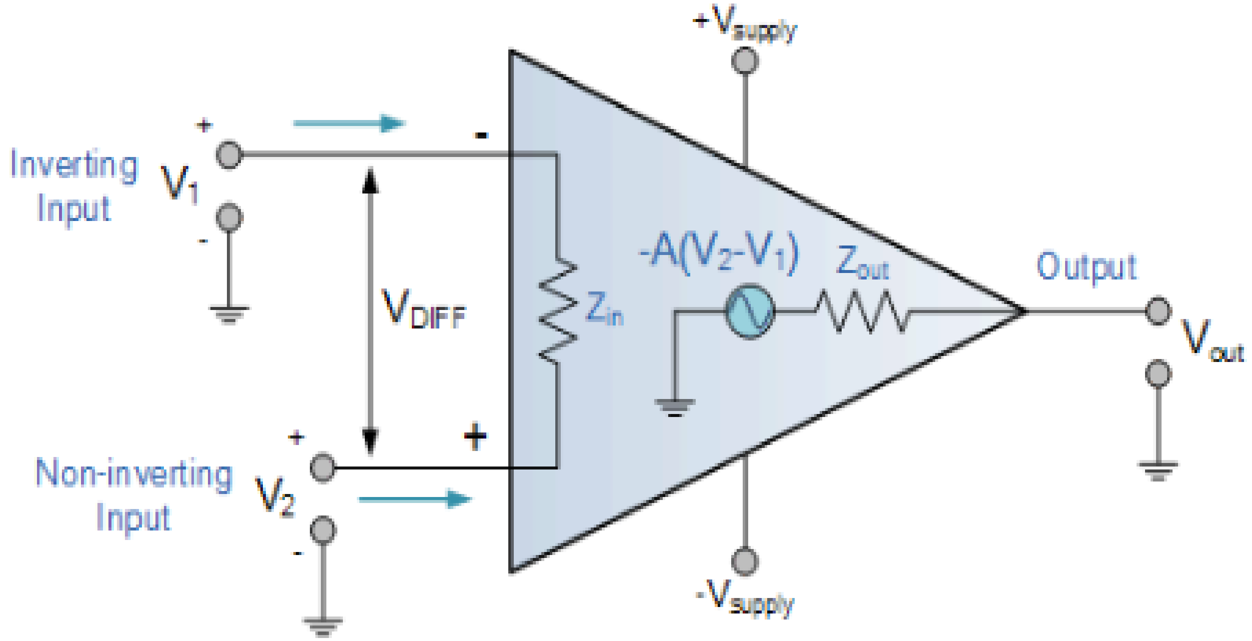
OPERATIONAL AMPLIFIERS

- Block schematic of an opamp:



- Voltage amplifying device designed to be used with external feedback components such as resistors and capacitors between its output and input terminals.
- Input stages - cascaded amplifiers(direct coupled DA) - provide high gain,high CMRR and high input impedance.
- Intermediate stage – high gain and frequency compensation (to give stabilityand no oscillation)
- Level shifter(adjusts the dc voltage so that o/p voltage is zero for zero inputs)
- Output stage-provides low output impedance(Class AB power amplifier) to prevent oscillations and unwanted signals within the amplifier
- An *Operational Amplifier* is basically a three-terminal device which consists of two high impedance inputs.
- One of the inputs is called the **Inverting Input**, marked with a negative or “minus” sign, (–).
- The other input is called the **Non-inverting Input**, marked with a positive or “plus” sign (+).
- A third terminal represents the operational amplifiers output port which can both sink and source either a voltage or a current.

EQUIVALENT CIRCUIT OF AN OPAMP



Vout=A Vid =A Vdiff=A(V1-V2)

where A-voltage gain

Vdiff-Difference i/p voltage

V1-Voltage at the non inverting terminal

V2-Voltage at the inverting terminal

VOLTAGE TRANSFER CURVE

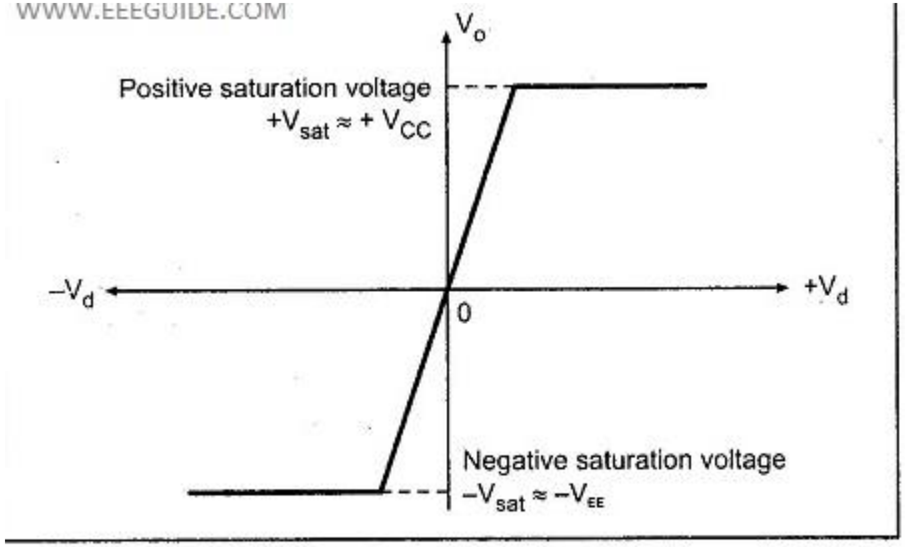


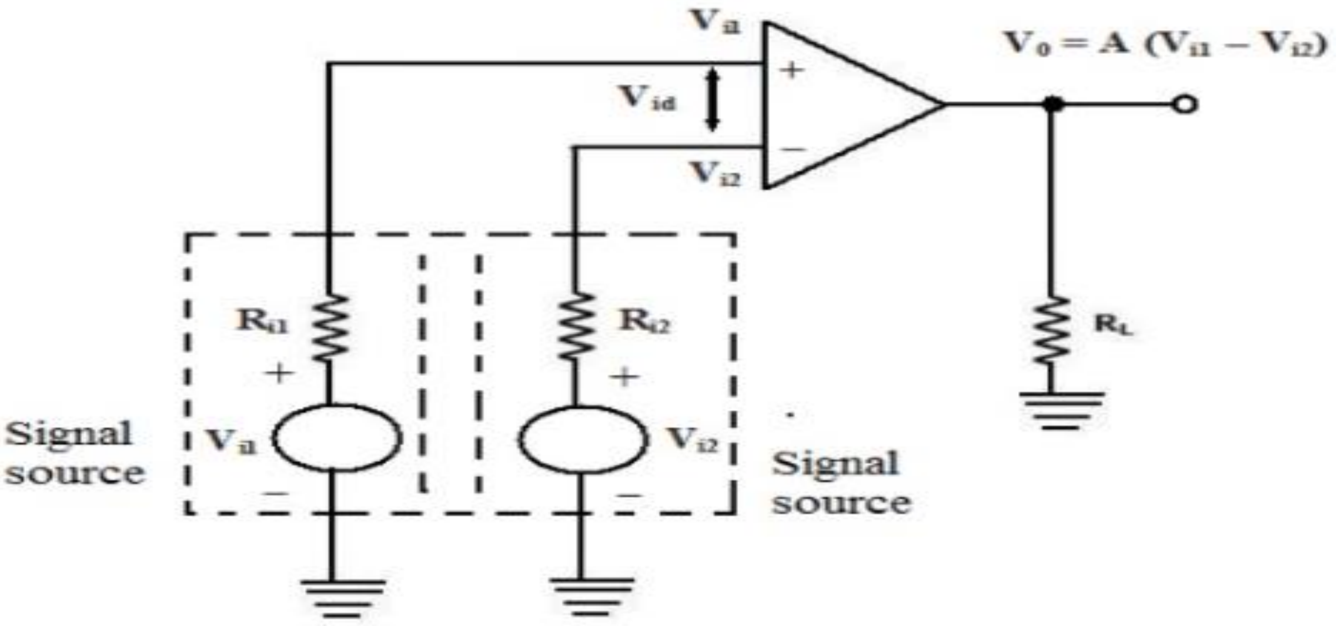
Fig. 2.7 Ideal voltage transfer curve

- Now the output voltage is proportional to difference input voltage but only upto the positive and negative saturation are specified by the manufacturer
- op-amp output voltage gets saturated at $+V_{cc}$ and – V_{ee} and it can not produce output voltage more than + V_{cc} and V_{ee} . Practically saturation voltages $+V_{sat}$, and $-V_{sat}$ are slightly less than $+V_{cc}$ and – V_{ee} .

APPLICATIONS OF OPAMPS

- Used in 2 modes:Openloop and Closed loop(connection between input and output

(a)Open loop configuration-no connection exists between input and output terminals

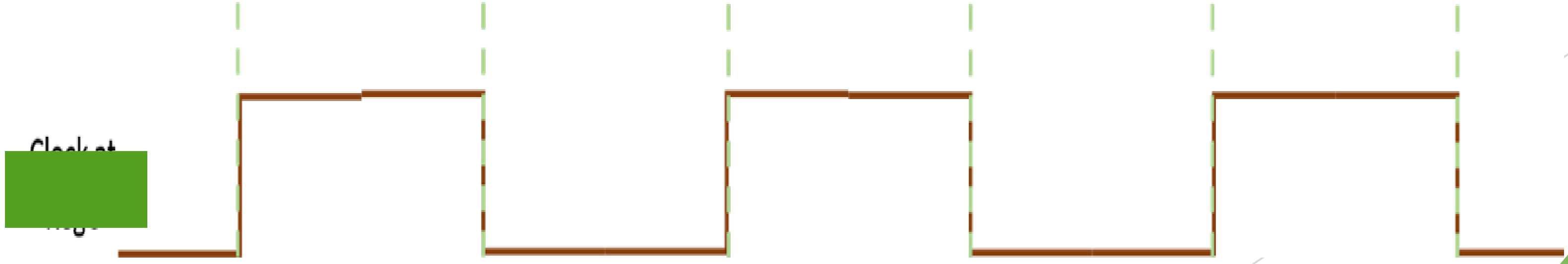


Open - loop Differential Amplifier

Ri1 and Ri2

Vo=A(Vi1-Vi2)

V1<V2

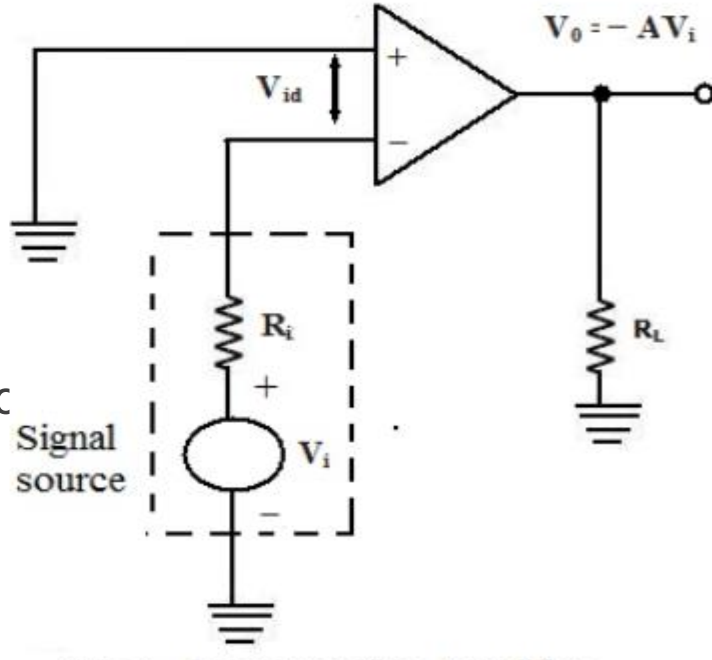


OPEN LOOP CONFIGURATIONS

- INVERTING AMPLIFIER
- The output voltage is 180^0 out of phase with respect to the input and

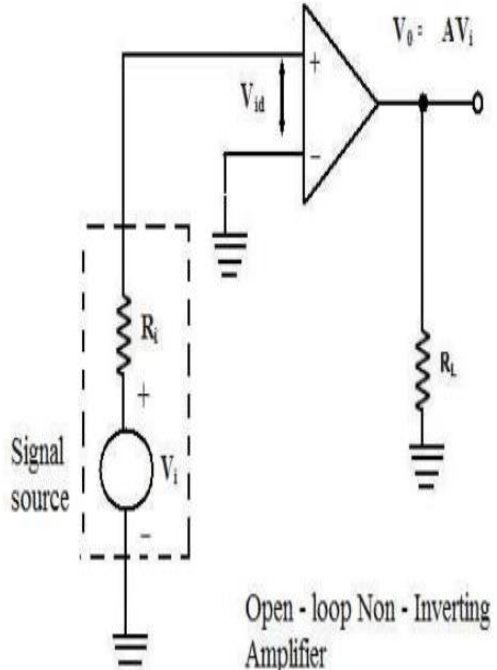
hence, the output voltage V0 is given by, $V_0 = -AV_i$

- Thus, in an inverting amplifier, the input signal is amplified by the open-loc gain A and in phase shifted by 180^0.



Open - loop Inverting Amplifier

- NON INVERTING AMPLIFIER
- The input signal is amplified by the open – loop gain A and the output is in-phase with input signal.
- In all the above open-loop configurations, only very small values of input voltages can be applied.
- Voltages levels slightly greater than zero, the output is driven into saturation
- When operated in the open-loop configuration, the output of the op-amp is either in negative or positive saturation, or switches between positive and negative saturation levels.
- This prevents the use of open – loop configuration of op-amps in linear applications.



Open - loop Non - Inverting Amplifier

LIMITATIONS

1. Clipping of the output waveform can occur when the output voltage exceeds the saturation level of op-amp. This is due to the very high open – loop gain of the op-amp.

- This feature actually makes it possible to amplify very low frequency signal and the amplification can be achieved accurately without any distortion.

2. The open – loop gain of the op – amp is not a constant and it varies with changing temperature and variations in power supply.

- The bandwidth of most of the open- loop op amps is negligibly small.

Continued…..

- Adm=(Vo1-Vo2)/VdVd=V1-V2(difference voltage)
- Acm=Vo1/Vc=Vo2/VcVc=common voltage(applied as inputs of both transistors)

CHARACTERISTICS OF OPAMPS:

INPUT BIAS CURRENT(Ib)

- It is the average value of the base currents entering into the terminals of opamp

Ib=(Ib1+Ib2)/2

Ib=500nA maximum for 741 IC

INPUT OFFSET CURRENT(Iio)

- Algebraic difference between the currents entering into the inverting and non inverting terminal

Iio=|Ib1-Ib2|

Iio=200nA maximum for 741 IC

INPUT OFFSET VOLTAGE(Vio)

- Voltage that must be applied at the input terminal of an opamp to make the output voltage zero.Voltage must be +ve/-ve

Continued….

CMRR(COMMON MODE REJECTION RATIO)

- Ratio of differential mode gain to the common mode gain.

CMRR= $\frac{|Adm|}{|Acm|}$,Maximum value=90dB

SLEW RATE

- Maximum rate of change of output voltage per unit of time and is expressed as Volt/micro seconds.

SR=$\frac{dVo}{dt}$

Indicates how rapidly the o/p of an opamp can change in response to changes in input frequency.

BANDWIDTH/GAIN BANDWIDTH PRODUCT

- It is the bandwidth of the opamp when the voltage gain is 1.

BW=1MHz

Infinite – The main function of an operational amplifier is to amplify the input signal and the more open loop gain it has the better. Open-loop gain is the gain of the op-amp without positive or negative feedback and for such an amplifier the gain will be infinite but typical real values range from about 20,000 to 200,000.

Input impedance, (Z_{IN})

Infinite – Input impedance is the ratio of input voltage to input current and is assumed to be infinite to prevent any current flowing from the source supply into the amplifiers input circuitry ($I_{IN} = 0$). Real op-amps have input leakage currents from a few pico-amps to a few milli-amps.

Output impedance, (Z_{OUT})

Zero – The output impedance of the ideal operational amplifier is assumed to be zero acting as a perfect internal voltage source with no internal resistance so that it can supply as much current as necessary to the load. This internal resistance is effectively in series with the load thereby reducing the output voltage available to the load. Real op-amps have output impedances in the 100-20kΩ range.

Bandwidth, (BW)

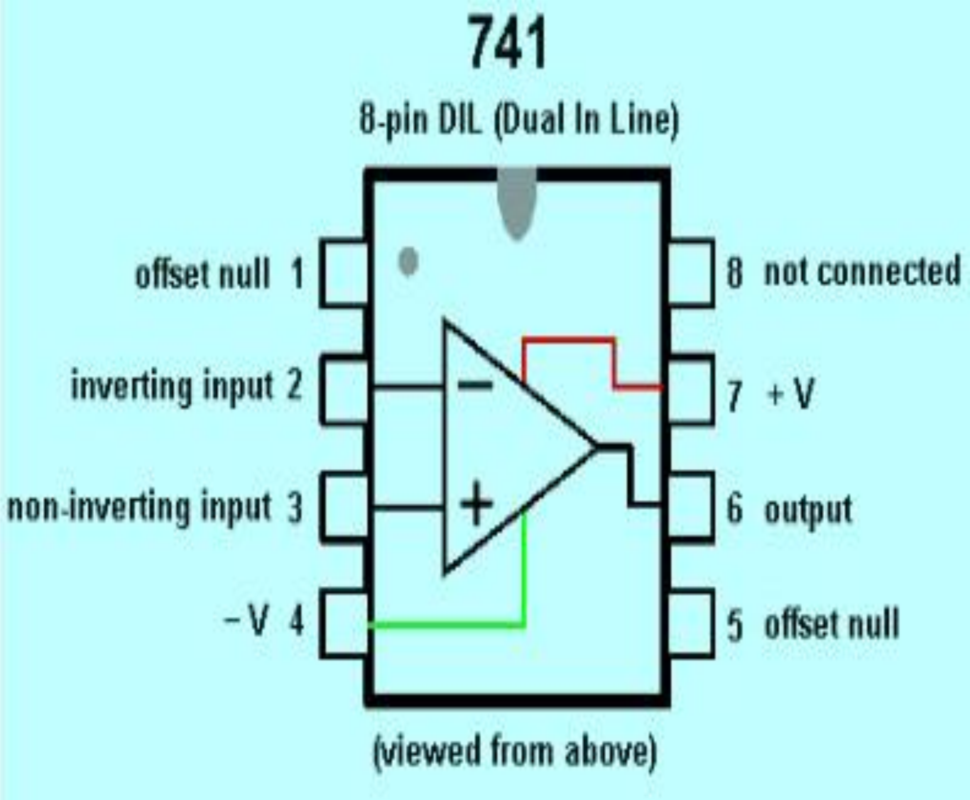
Infinite – An ideal operational amplifier has an infinite frequency response and can amplify any frequency signal from DC to the highest AC frequencies so it is therefore assumed to have an infinite bandwidth. With real op-amps, the bandwidth is limited by the Gain-Bandwidth product (GB), which is equal to the frequency where the amplifiers gain becomes unity.

Offset Voltage, (V_{IO})

Zero – The amplifiers output will be zero when the voltage difference between the inverting and the non-inverting inputs is zero, the same or when both inputs are grounded. Real op-amps have some amount of output offset voltage.

IDEAL CHARACTERISTICS OF OPAMP

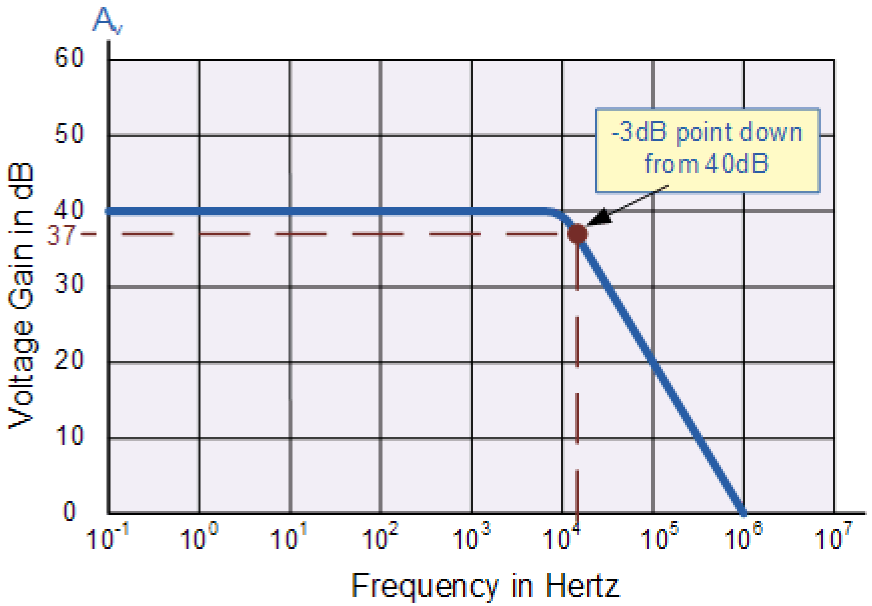
- Infinite voltage gain
- Infinite input resistance
- Zero output resistance
- Zero output voltage when input voltage is zero
- Infinite Bandwidth
- Infinite CMRR
- Infinite Slewrate



COMPARISON OF IDEAL AND PRACTICAL OPAMP(741 IC)

Ideal	Practical
• Infinite voltage gain • Infinite input resistance • Zero o/p resistance • Infinite bandwidth • Infinite CMRR • Infinite slewrate • Zero o/p voltage when i/p =0	• Voltage gain is 200,000 • Input resistance 2MΩ • O/p resistance 75 Ω • Bandwidth is 1 MHz • CMRR is 90 dB • Slewrate is 0.5V/μs • Not able to get zero at the o/p when i/p=o due to mismatch in transistors

FREQUENCY RESPONSE-CALCULATION OF BANDWIDTH



BW=0.35/Rise time

BW=A*f

- The operational amplifiers bandwidth is the frequency range over which the voltage gain of the amplifier is above **70.7%** or **-3dB** (where 0dB is the maximum) of its maximum output value
- Problem 1:GBP of the amplifier, in this particular case 1MHz. calculate the bandwidth of the amplifier
- 37=20logA=➔A=antilog (37 ÷ 20) = 70.8
- GBP ÷ A = Bandwidth, therefore, 1,000,000 ÷ 70.8 = 14,124Hz, or 14kHz
- Problem 2:*If* the -3dB point would now be at 17dB.Find BW.

CALCULATION OF SLEW RATE

- Slew rate=$\frac{dVo}{dt}$|max
- If Vo=Vm Sinwt,$\frac{dVo}{dt}$=w Vm cos wt
- At max,wVm=2ΠfVm
- Typical Value=1V/μs=10^6V/s

1.If f=1KHz,find Vm

Ans:Vm=$\frac{10^6}{2\pi f}$=16V

Problems:

1.An opamp has unity gain frequency of 100kHz.If an amplifier has a gain of 10 is needed,what can be its-3dB cut off frequency.

Ans:fu=100*10^3=A*fc

$$fc=\frac{100*10^3}{10}=10kHz$$

2.An opamp has a slew rate of 2V/µs.What is the maximum closed loop voltage gain that can be obtained if the input signal varies by 0.5Vpp in 10µs.

Ans:SR=2V/µs,i/p voltage=0.5V in 10µs

$$\frac{2}{10^{-6}}=\frac{0.5*Acl}{10*10^{-6}}$$

Acl=2/0.05=40 (Vid=Vm/A)

3.An opamp has a slewrate of 1V/µs,a unity gain frequency of 1MHz.O/p saturation level is 12V.Calculate maximum frequency.Calculate the maximum peak amplitude of input sinusoidal frequency 100KHz.

Ans:$fmax=\frac{SR}{2*\pi*Vm}$

$$fmax=\frac{SR}{2*\pi*Vm}=\frac{1V}{10^{-6}*2\pi*12}=13.263kHz$$

$fmax=\frac{SR}{2*\pi*Vm}$ 100*10^3=$\frac{1V}{10^{-6}*2\pi*Vm}$;Vm=1.592V

Continued….

4.Output voltage of an opamp circuit changes by 20V in 4μs.What is the slew rate?

Ans:Slew rate=$\frac{dVo}{dt}$|max =$\frac{20V}{4*10^{-6}}$=5V/μs

5.An inverting amplifier with opamp has a gain of 50.Maximum amplitude of 20mV.What is the maximum frequency of the input at which the output will be undistorted?

Ans:SR=$\frac{2*\pi*f*Vm}{10^6}$=0.5

Vm=A*Vid

=50*20*10^{-3}=1V

fmax=$\frac{SR*10^6}{2*\pi*Vm} = \frac{0.5*10^6}{2*\pi*1}$=79.6kHz

6. With the help of a circuit diagram explain the working of a differential amplifier if the following inputs are applied (i) Vb1=0V, Vb2=1V (ii) Vb1=1V, Vb2=1V (iii) Vb1= -1V, Vb2=1V

7. For a differential amplifier, find the value of Vid to cause iE2= 0.98*I where Vid = VB1- VB2 and I is the tail current.

8. List out the ideal characteristics of an op.amp

9. Draw the block diagram and equivalent circuit of an operational amplifier.

10. With the help of a circuit diagram, derive the equation for Input differential resistance of a differential amplifier

Continued…..

11. Explain the openloop configurations and voltage transfer curve of an ideal opamp

12. Explain the following properties of a practical opamp (i) Bandwidth (ii) Slew rate (iii) Input offset voltage (iv) Input offset current

13. Define slew rate. What are its causes? Derive the equation for maximum input frequency at which an undistorted signal is obtained in terms of slew rate?

14. Analyse the BJT differential amplifier pair under large signal operation and illustrate its transfer characteristics.

15. Using the small signal analysis, deduce the expression for CMRR

16. What is the principle of operation of Wilson current mirror and its advantages? Deduce the expression for its current gain.