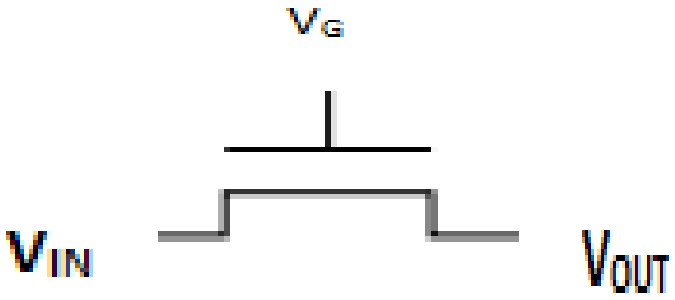
EC 304 - VLSI

Module IV

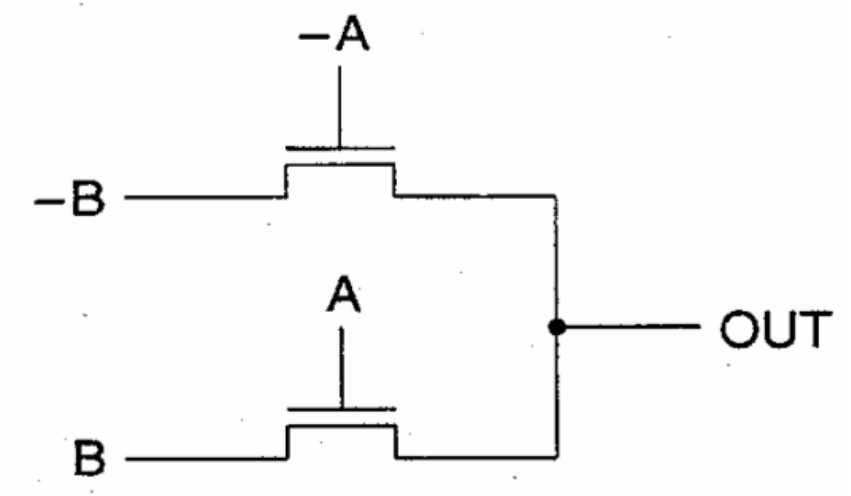
PASS TRANSISTOR

- They are simple FETs that pass the signal between the drain and source terminals instead of a fixed power supply value
- The switch is controlled by the gate voltage V_G
- If V_G =0, then the transistor is OFF and there is no connection between the input and output
- Placing a high voltage of $V_G = V_{DD}$ drives the nFET active and current can flow

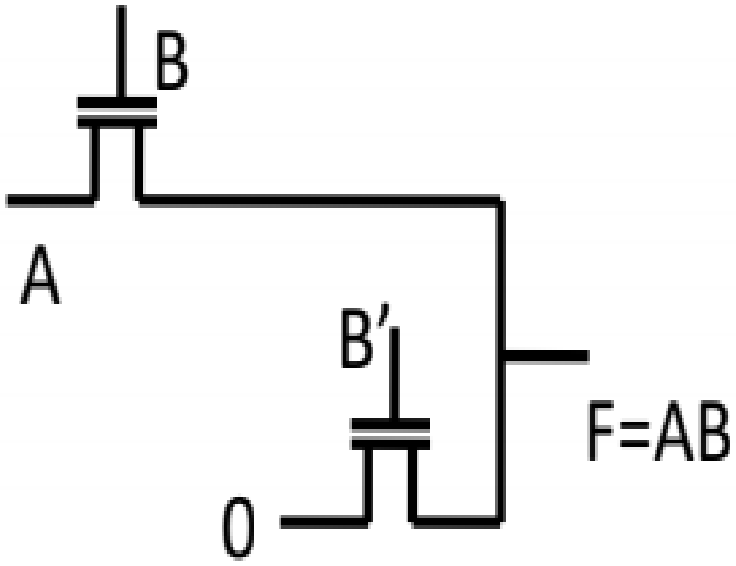


XNOR implementation

- If A is high, B is passed through the gate to the output
- If A is low, -B is passed through the gate to the output

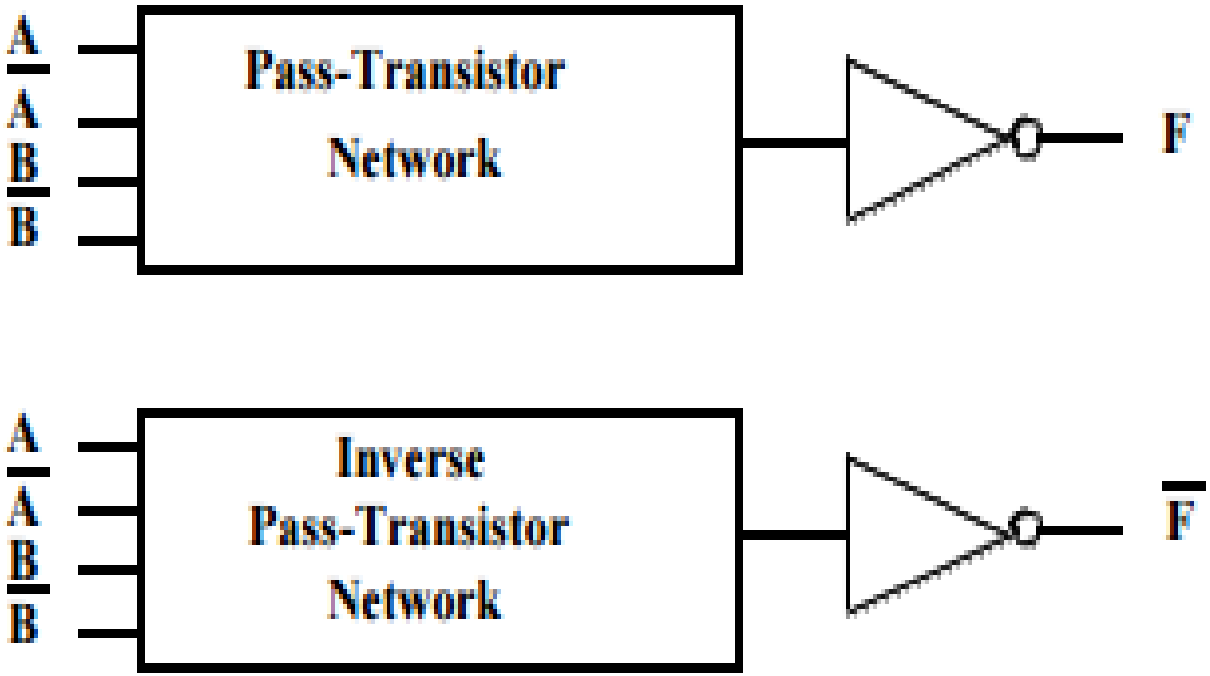


AND Implementation



- **Advantage**
  - Less number of transistors
- **Disadvantage**
  - NMOS is effective in passing 0 but poor in pulling a node to VDD. Hence, in a NMOS based pass transistor the high output is VDD-VT instead of VDD.
  - Cascading is not possible

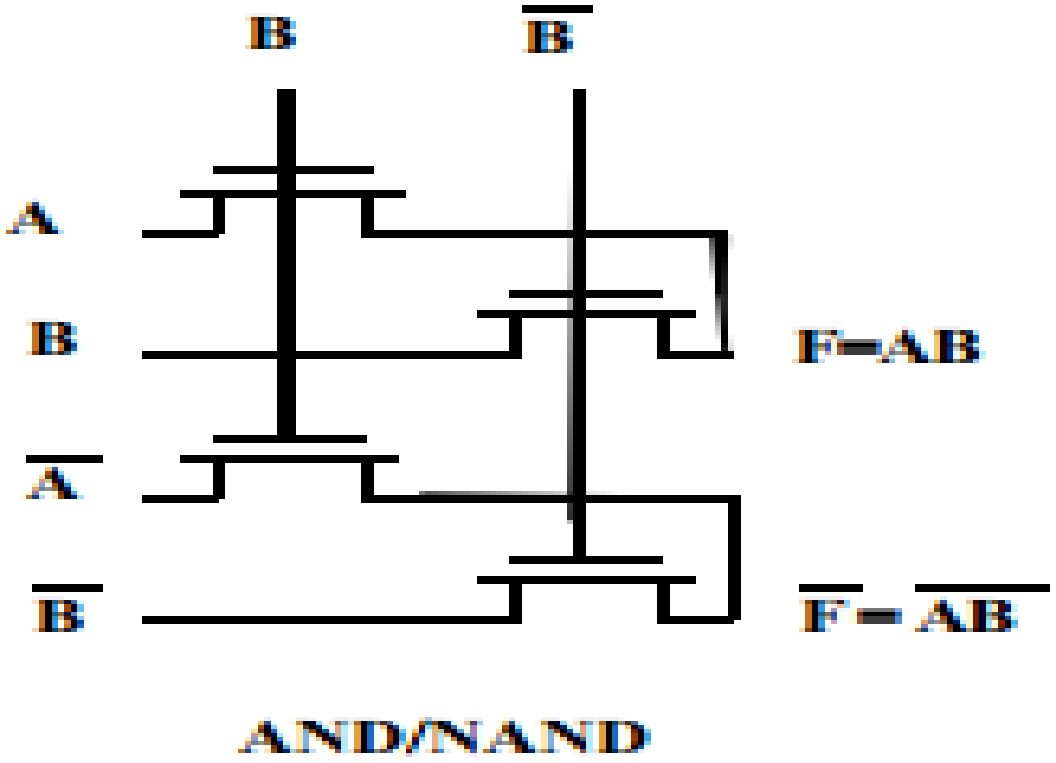
Differential pass transistor logic



CPL / DPL

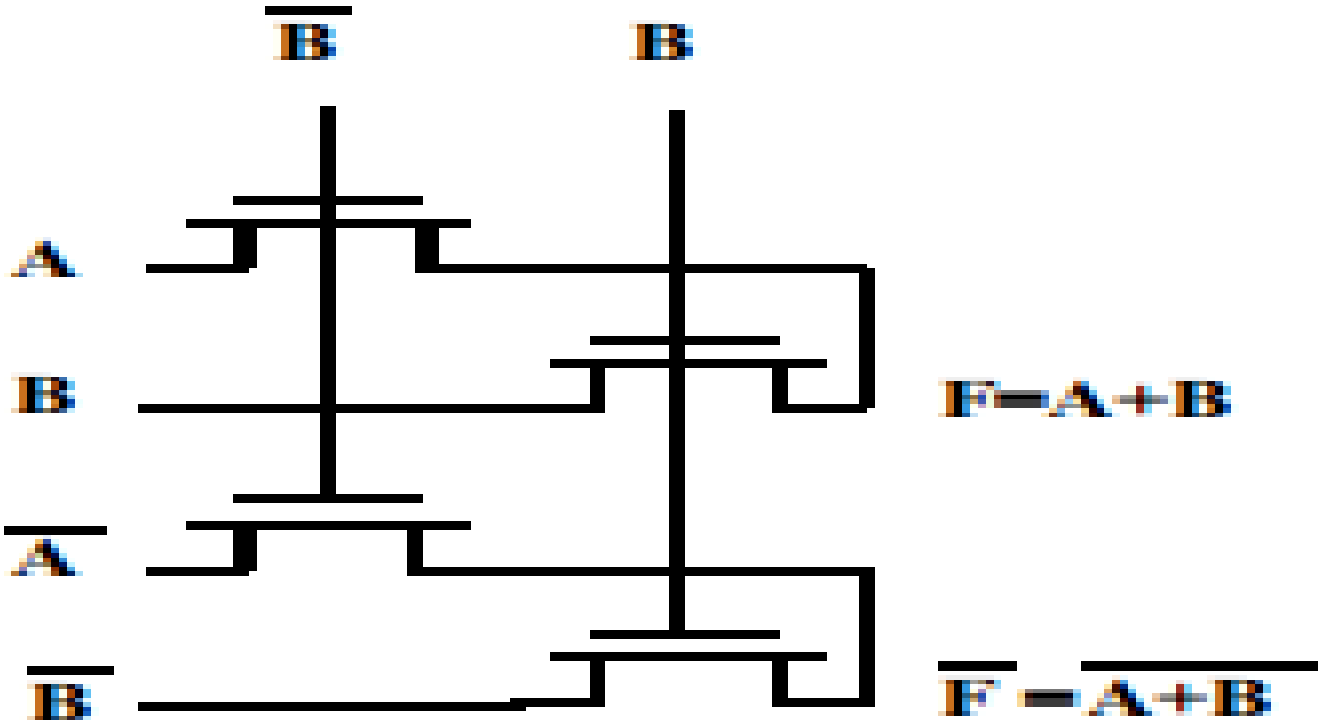
- Designed for high performance
- Accept true and complementary inputs and produce true and complementary outputs
- Since the circuits are differential complementary data inputs and outputs are always available
- Since circuit is differential, complimentary inputs and outputs are available.
- Although generating differential signals require extra circuitry, complex gates such as XORs, MUXs and adders can be realized efficiently.
- CPL is a static gate, because outputs are connected to V_{DD} or GND through a low-resistance path (high noise resilience).
- Design is modular – all gates use same topology; only inputs are permuted. This facilitates the design of a library of gates

AND/NAND



AND/NAND

OR/ NOR


$\overline{B}$
B
A
B
$\overline{A}$
$\overline{B}$
F=A+B
$\overline{F} = \overline{A+B}$

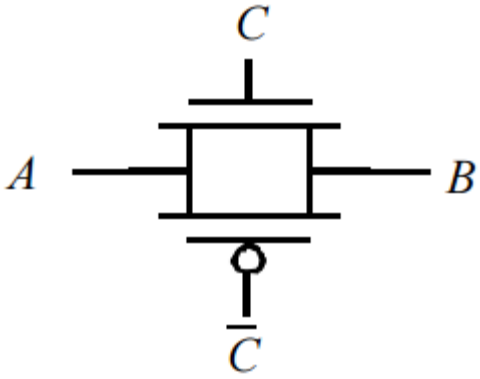
OR/NOR

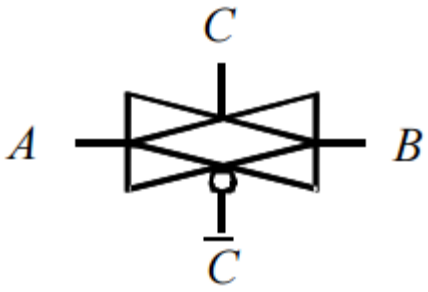
- Differential pass-transistor logic suffers from the problem of
  - ✓Static power dissipation
  - ✓Reduced noise margin.
- There are several solutions are proposed to deal with such problems-

1. **Level Restoration**
2. **Multiple-Threshold Transistor**
3. **Transmission gate logic**

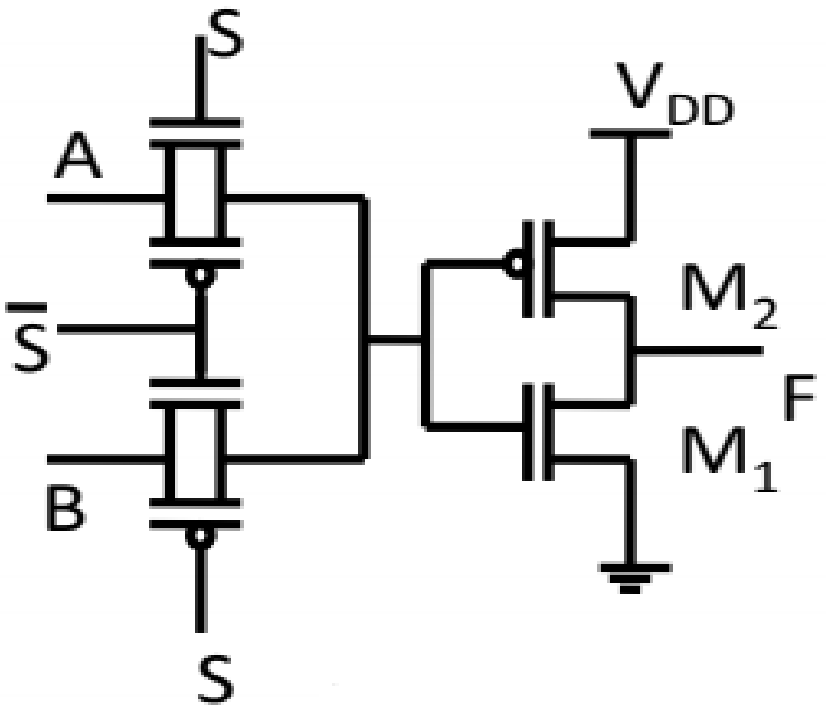
Transmission gates

- Uses the complementary property of NMOS and PMOS
- NMOS passes strong 0 and weak 1
- PMOS passes strong1 and weak 0
- Placing a NMOS in parallel with PMOS
- Control signals to transmission gate C and C
- It acts like a bidirectional switch controlled by a gate signal C
- Transmission gates can be used to build some complex gates very efficiently





Transmission Gate Multiplexer



THANK YOU