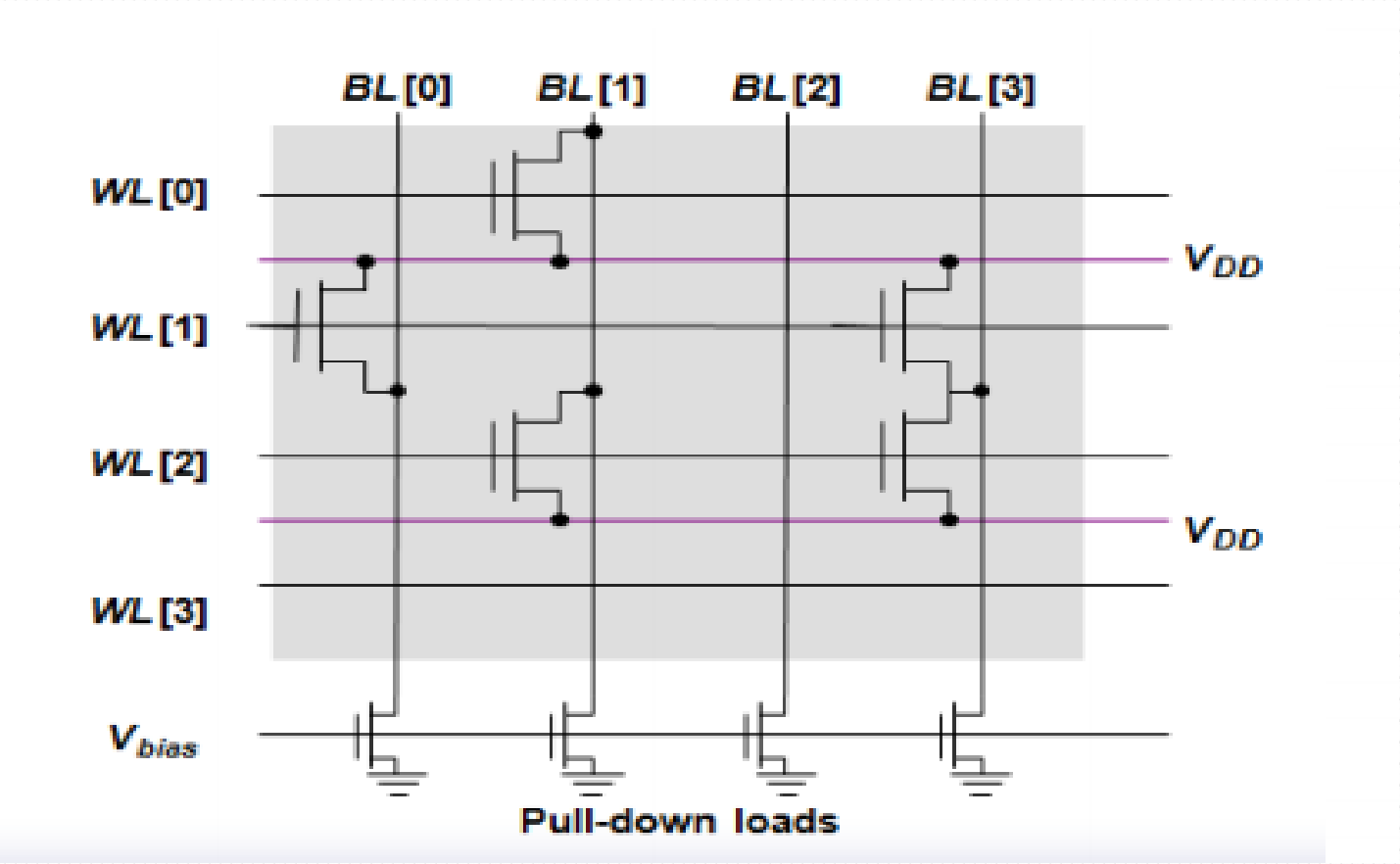
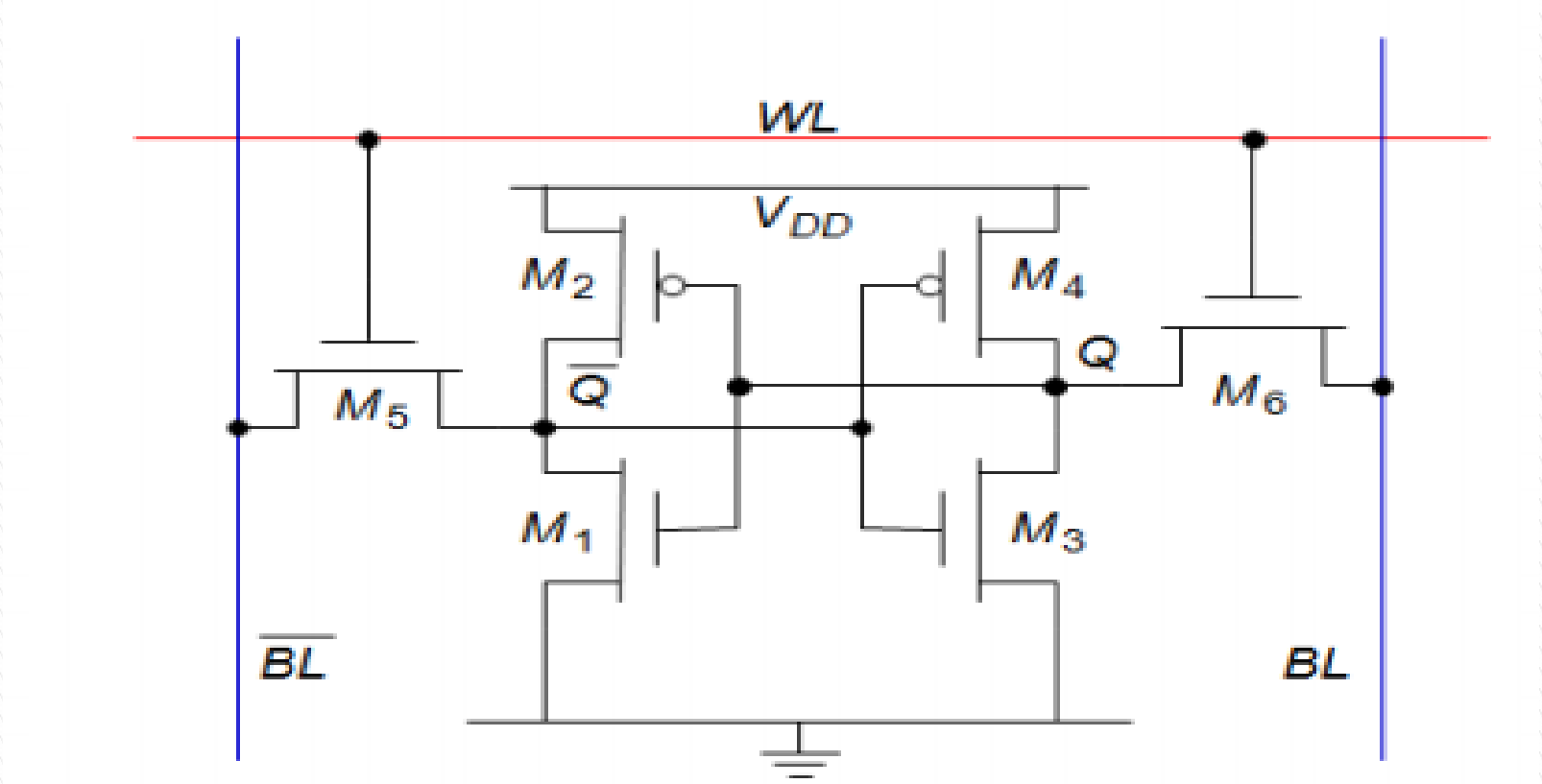
EC 304 – VLSI
Module V

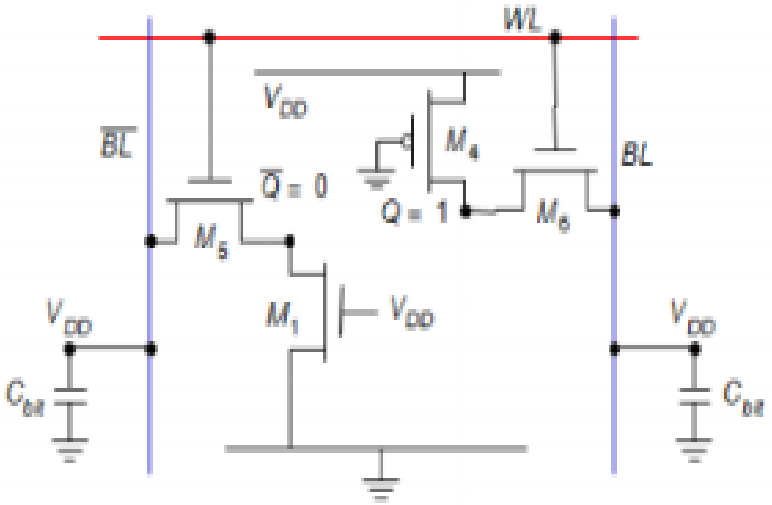
4 x 4 OR ROM Cell



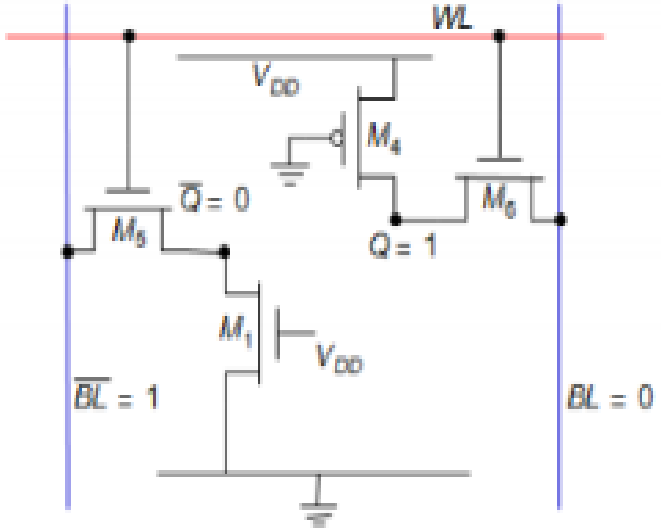
STATIC RAM



SRAM READ & WRITE OPERATION

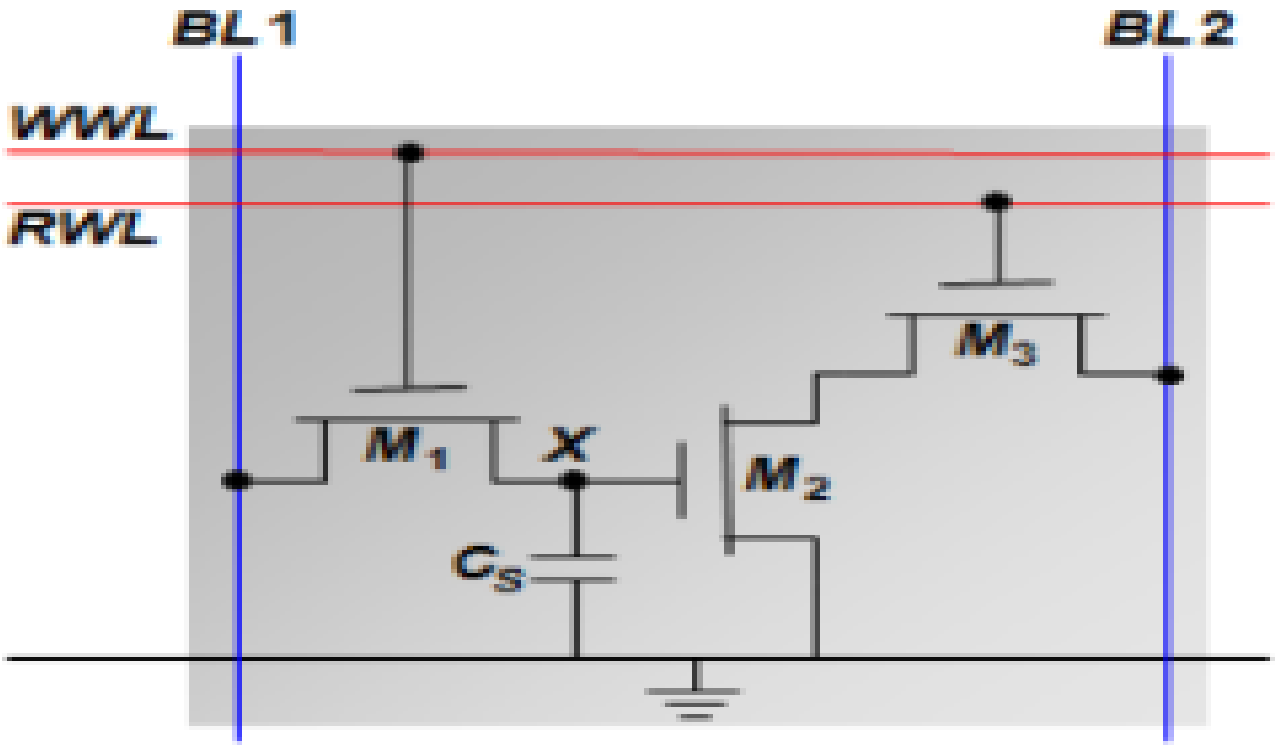


Read Operation

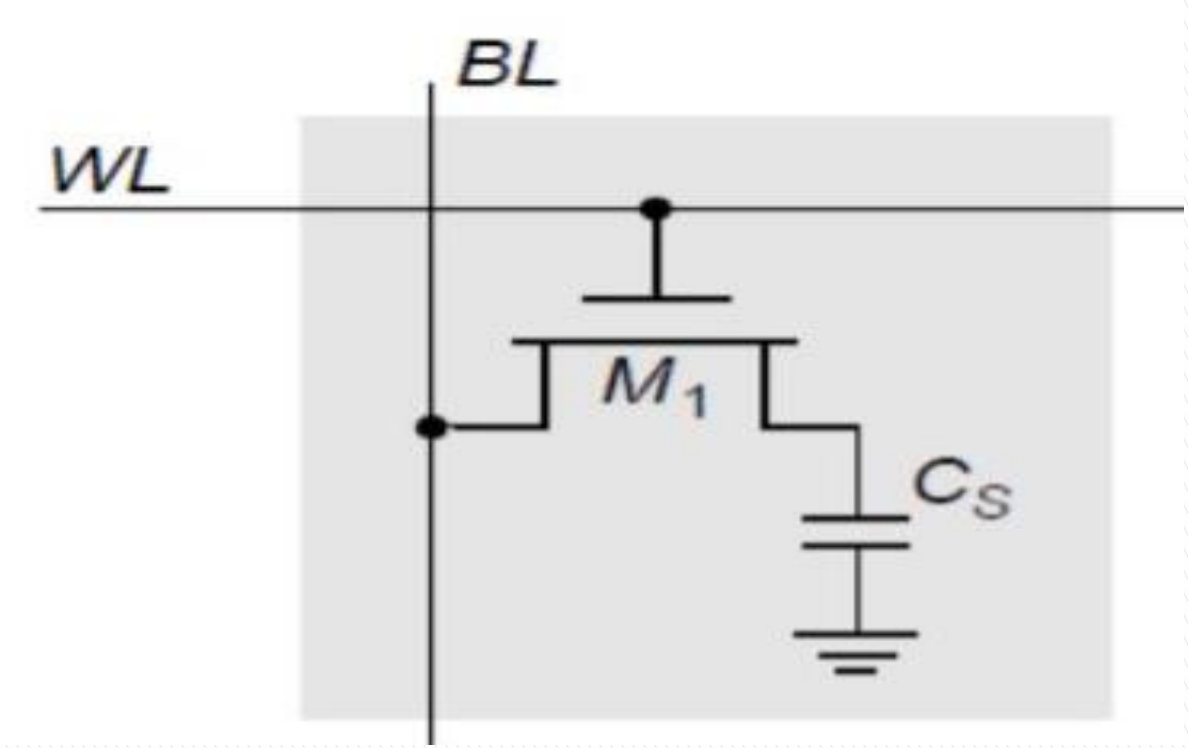


Write Operation

3T DRAM



1T DRAM



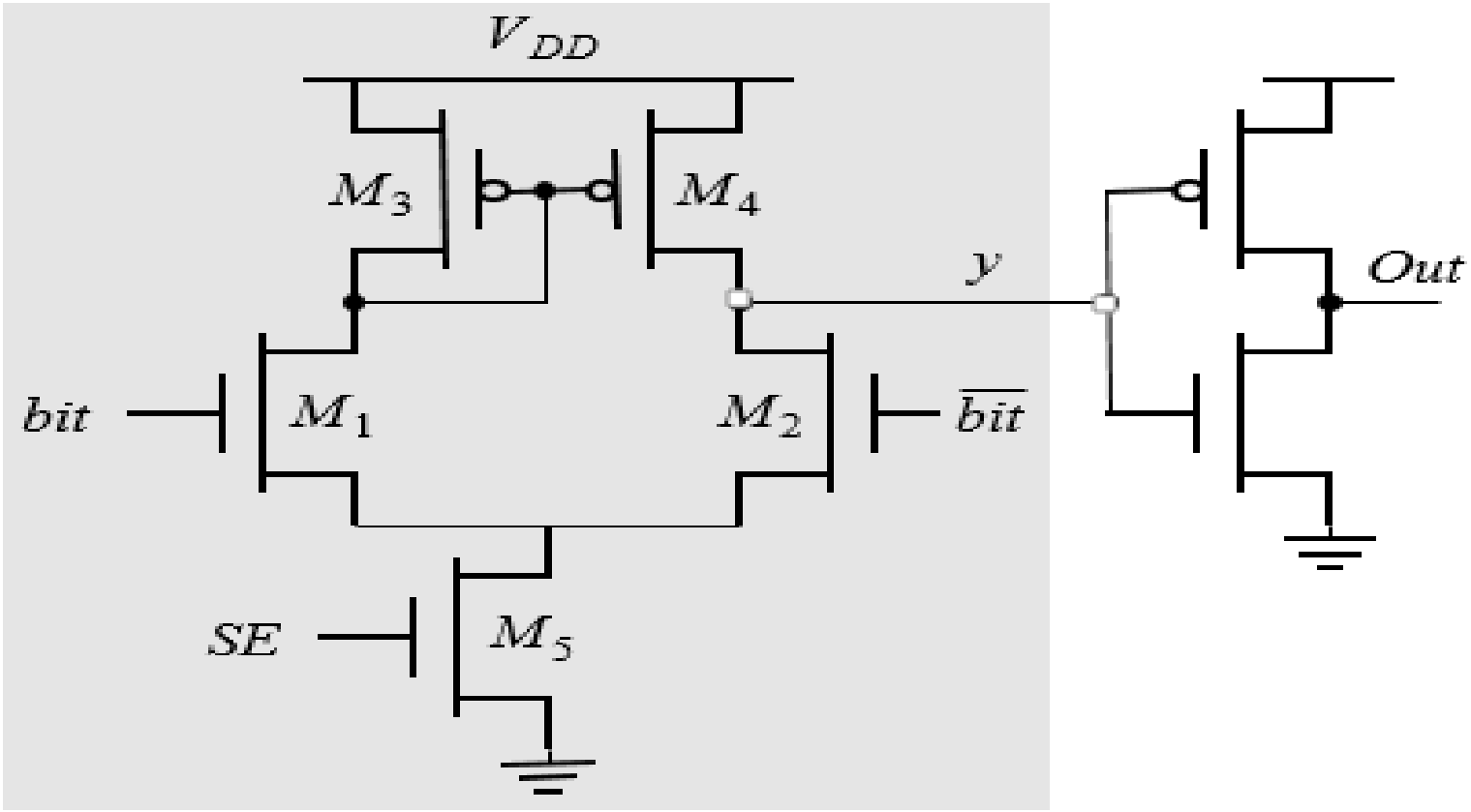
Sense Amplifier

- They are analog amplifiers by nature
- They play a major role in the functionality, performance and reliability of memory circuits
- Their main functions are:
- **Amplification** : In some memory structures like 1TDRAM, amplification is required for proper functionality since the typical circuit swing is limited to 100 millivolts
- **Delay reduction**: The amplifiers compensates for the restricted fan-out driving capability of the memory cell by accelerating the bit line transition or by detecting and amplifying small transitions on the bit line to large signal output swings.
- **Power reduction**: Reducing the signal swing on the bit lines can eliminate a substantial part of the power dissipation related to charging and discharging the bit lines
- **Signal restoration:** Because read and refresh functions are intrinsically linked in 1T DRAMs , it is necessary to drive the bit lines to the full signal range after sensing

Basic differential sense amplifier

- Amplification is accomplished with a single stage, based on the current mirroring concept
- The input signals (bit and bit) are heavily loaded and driven by the SRAM memory cell and the swing on these lines is very small as these drive a large capacitive load
- The inputs are fed to the differential input devices ($M_1$and M_2).
- M3and M4 act as an active current mirror load
- The amplifier is conditioned by the sense amplifier enable signal, SE

Differential Sense Amplifier



- Initially, the inputs are precharged and equalized to a common value, while SE is low disabling the sensing circuit
- Once the read operation is initiated , one of the bit lines drops.
- SE is enabled when a sufficient differential signal had been eastablised and the amplifier evaluates
- The gain of the differential to single ended amplifier is
- $A_{sense} = g_{m1}(r_{o2} \parallel r_{o4})$
- g_{m1} = transconductance of the input transistors
- r_0 = small signal device resistance of the transistor
- The main goal of the sense amplifier is the rapid production of an output signal

Types of Programmable Logic Devices

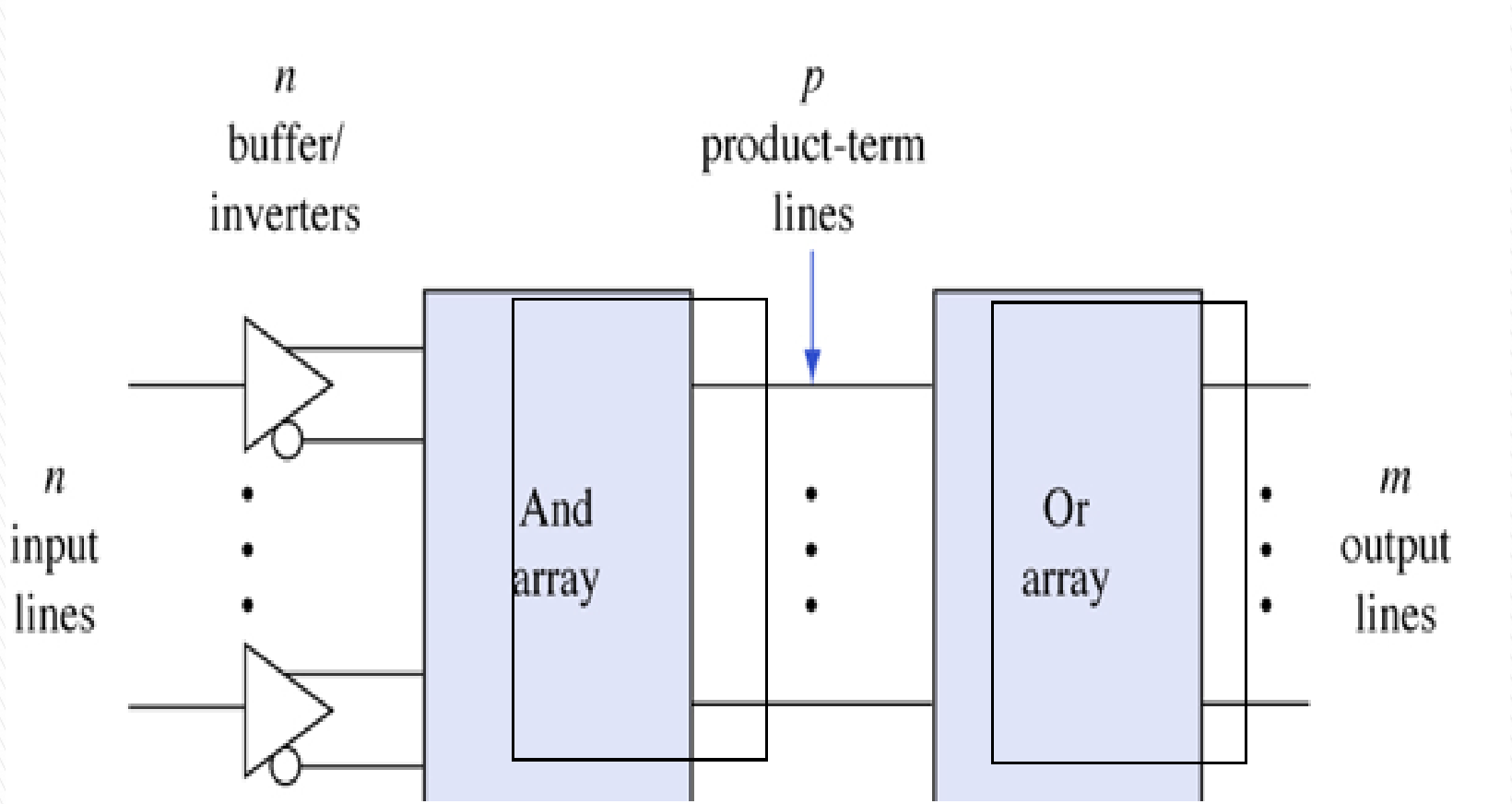
- SPLDs (Simple Programmable Logic Devices)
  - ROM (Read-Only Memory)
  - PLA (Programmable Logic Array)
  - PAL (Programmable Array Logic)
  - GAL (Generic Array Logic)
- CPLD (Complex Programmable Logic Device)
- FPGA (Field-Programmable Gate Array)

- The first three varieties are quite similar to each other:
  - They all have an input connection matrix, which connects the inputs of the device to an array of AND-gates.
  - They all have an output connection matrix, which connect the outputs of the AND-gates to the inputs of OR-gates which drive the outputs of the device.

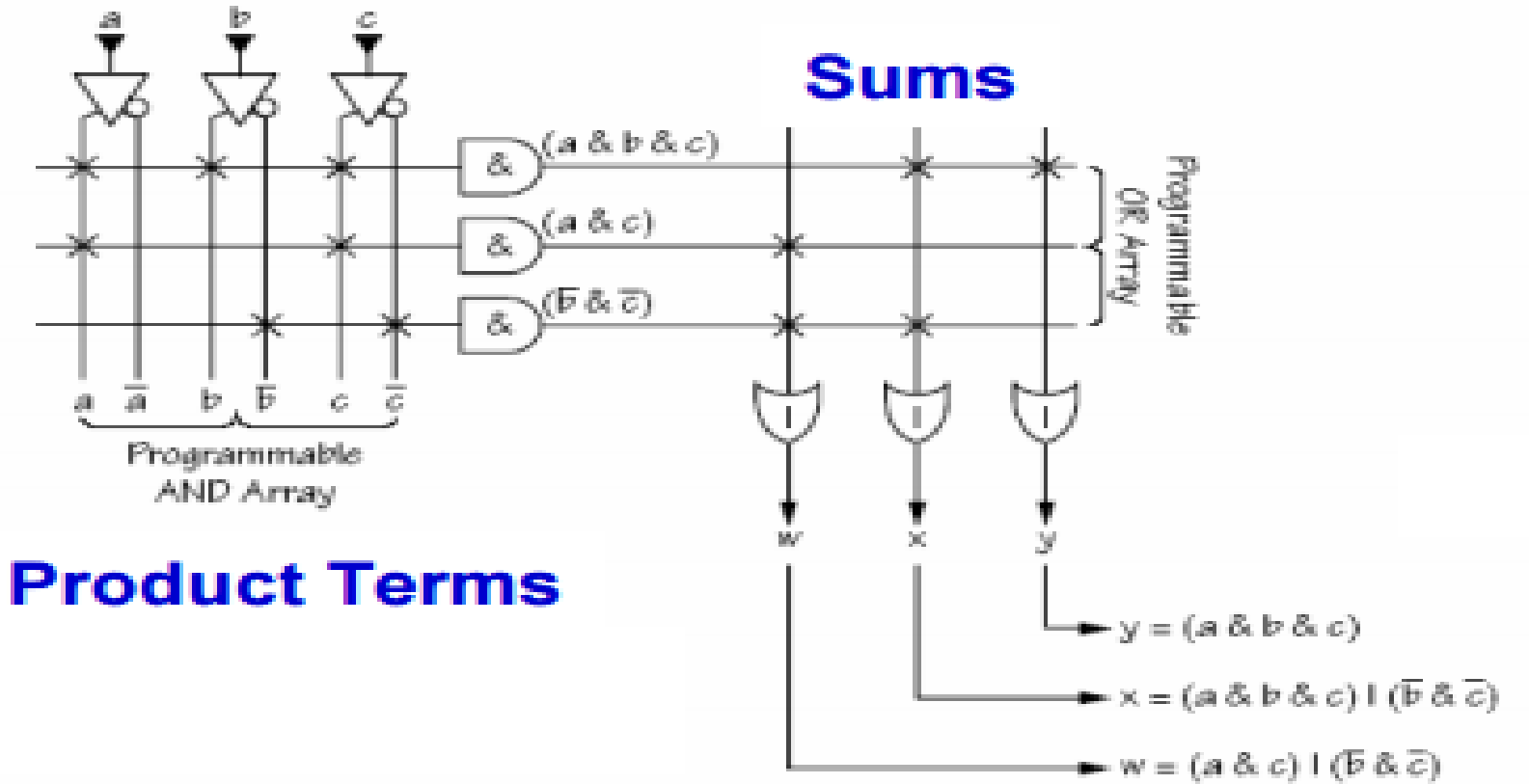
Comparison

Device	AND-array	OR-array
PROM	Fixed	Programmable
PLA	Programmable	Programmable
PAL	Programmable	Fixed
GAL	Programmable	Fixed

General structure of PLDs

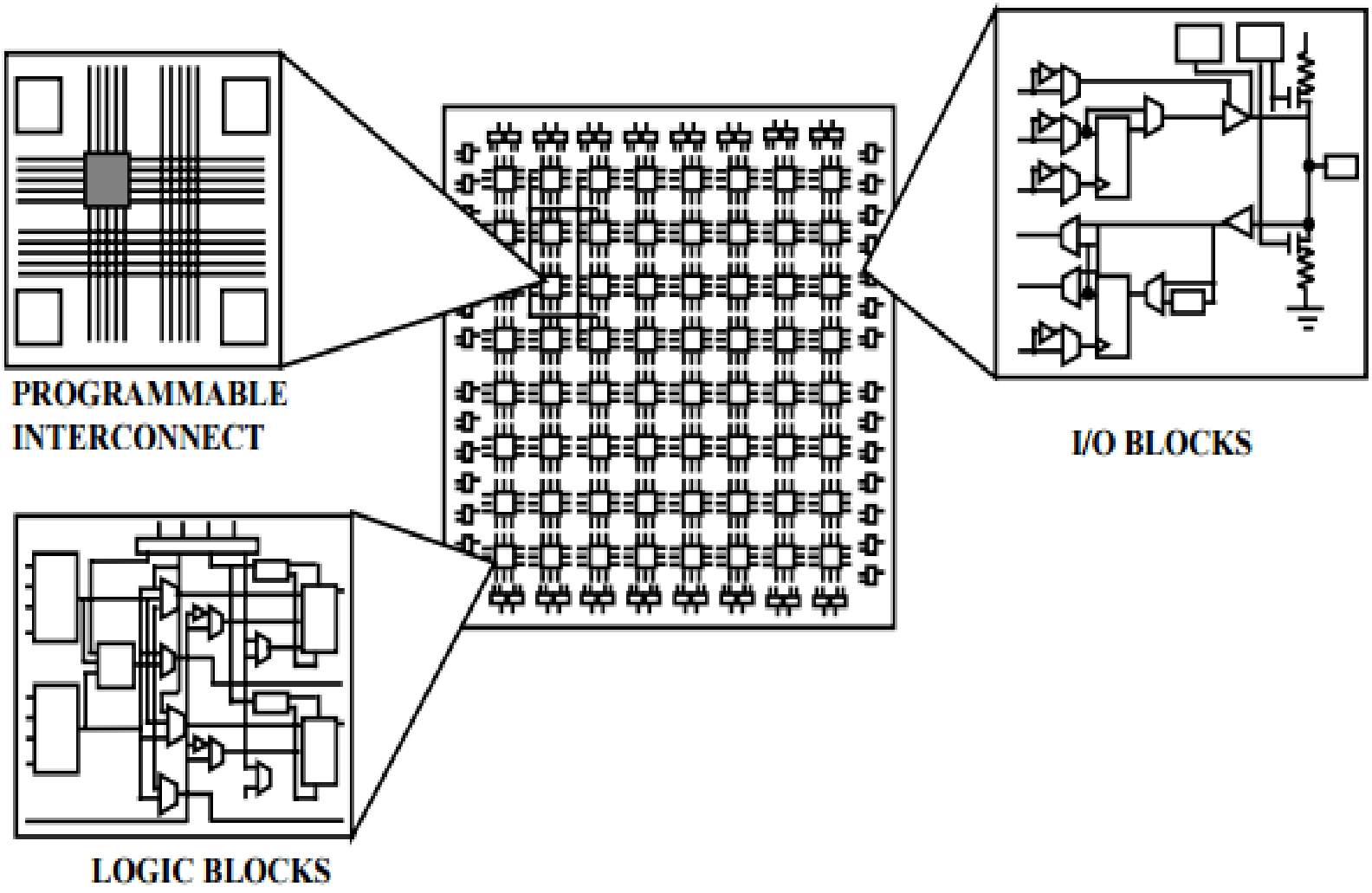


Programmable Logic Array



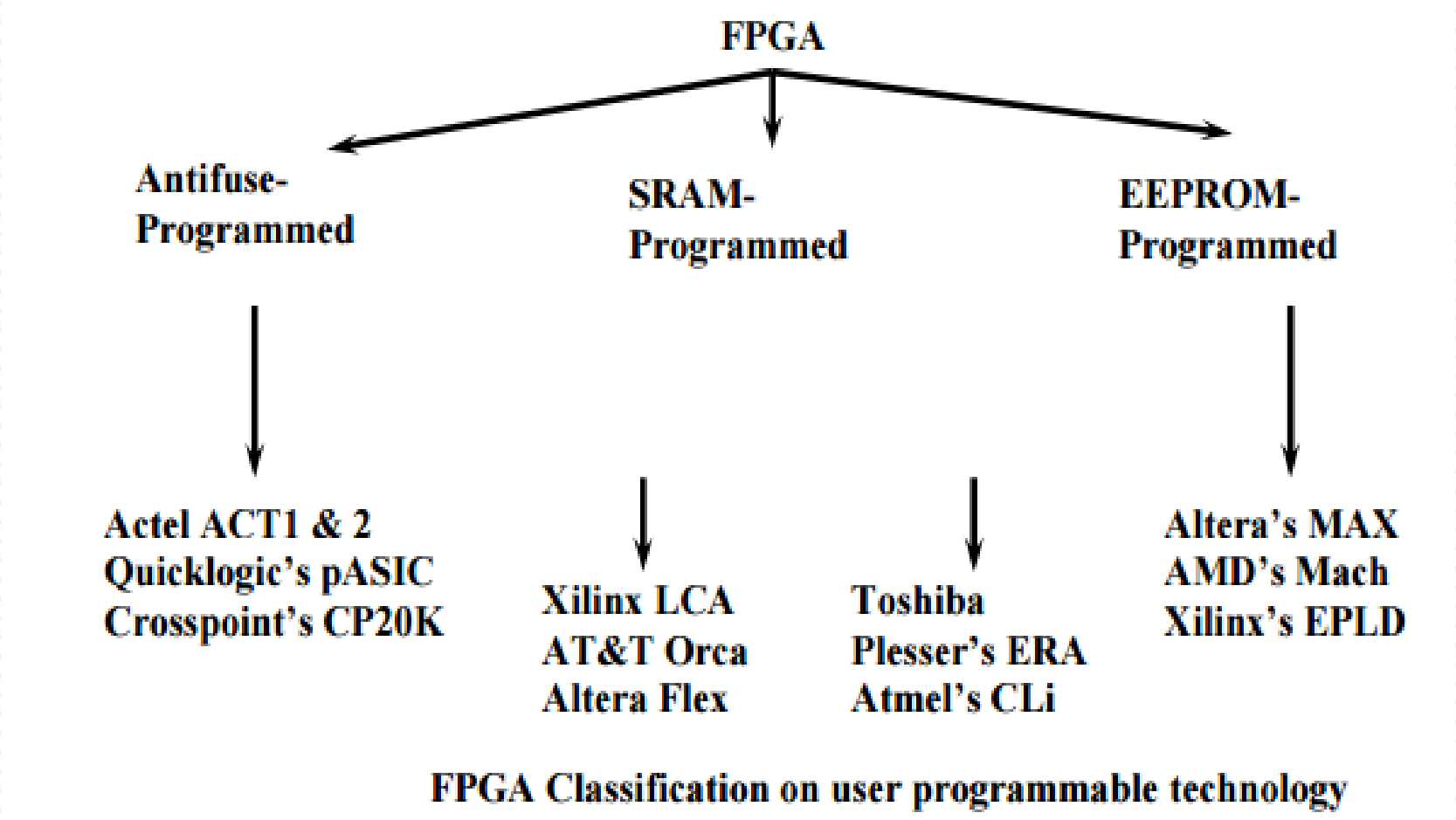
FIELD PROGRAMMABLE GATE ARRAY (FPGA)

- An FPGA is a device that contains a matrix of reconfigurable gate array logic circuitry.
- When a FPGA is configured, the internal circuitry is connected in a way that creates a hardware implementation of the software application.
- Unlike processors, FPGAs use dedicated hardware for processing logic and do not have an operating system.
- FPGA-based systems can literally rewire their internal circuitry to allow reconfiguration .
- FPGA devices deliver the performance and reliability of dedicated hardware circuitry.



Internal Structure of FPGA

FPGA Classification



FPGA Classification on user programmable technology