EC 464 – LPVLSI

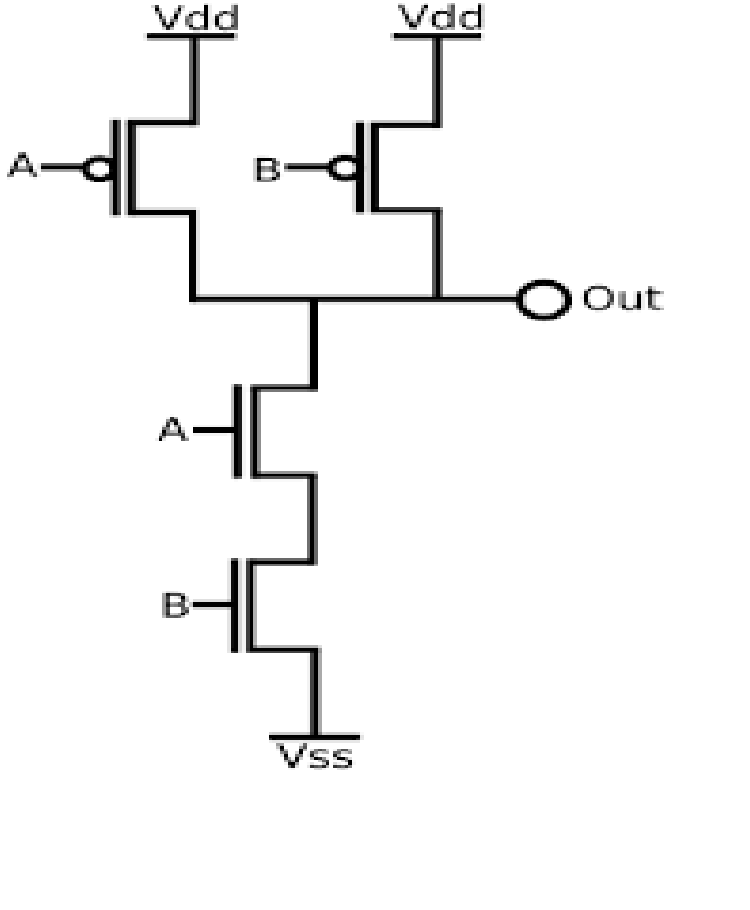
Module V

Fully Complementary Logic

- Advantages
  - Ease of design
  - Low power dissipation
  - Low sensitivity of noise
  - Scalability
- Disadvantages
  - Low performance for large fan in gates

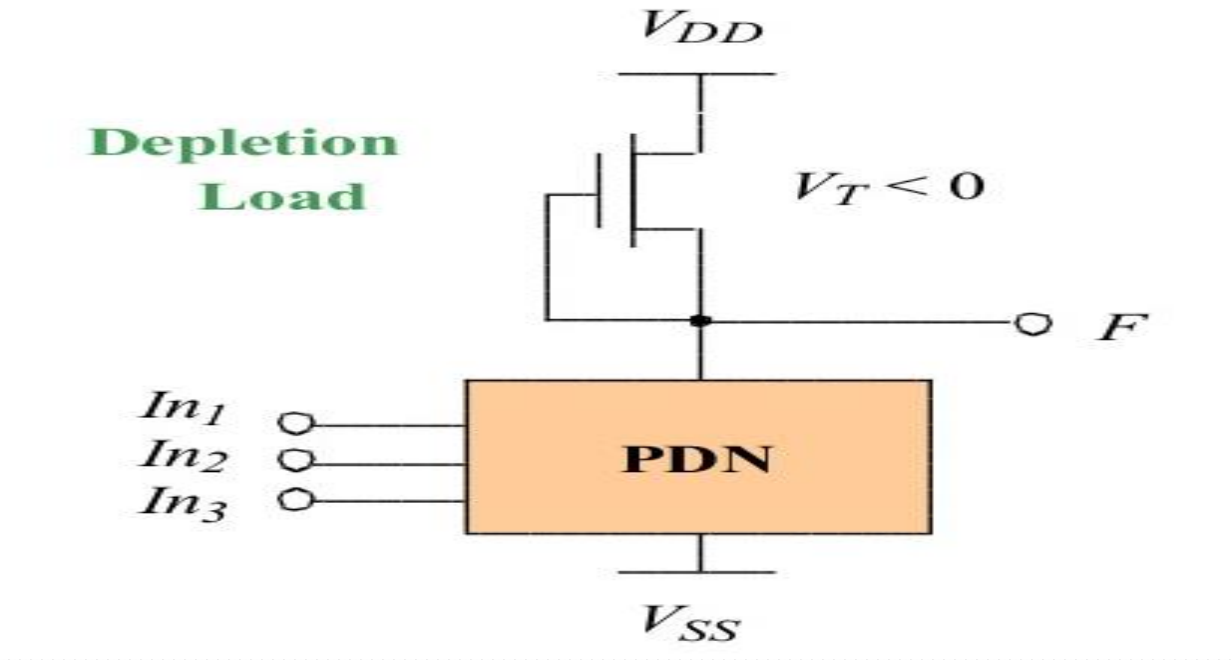
- Requires 2N transistors for N input logic
  - N NMOS
  - N PMOS

2 input NAND

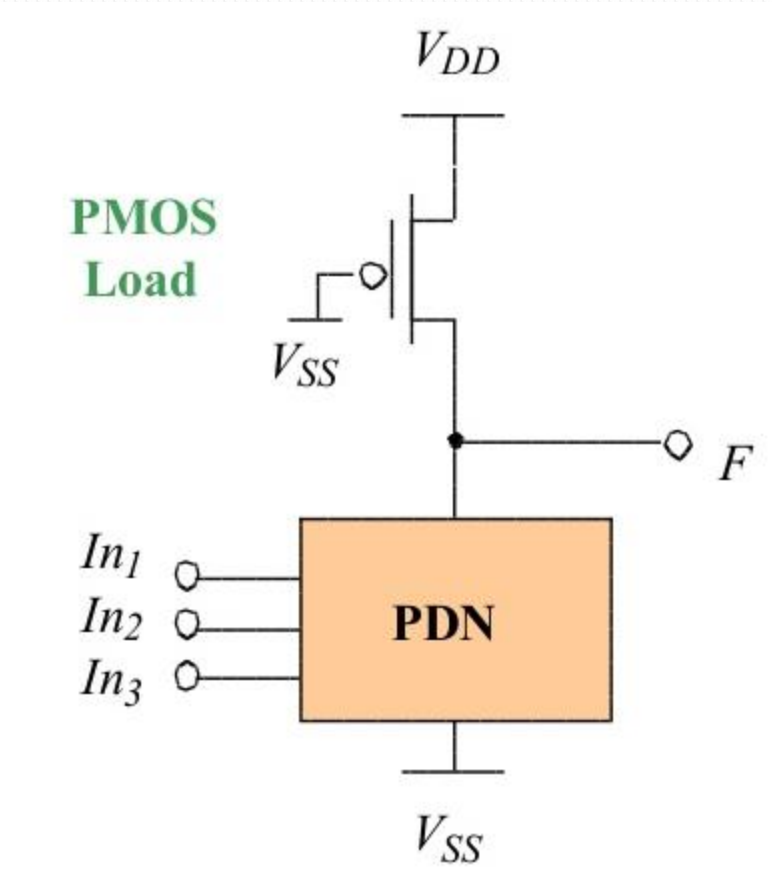


A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

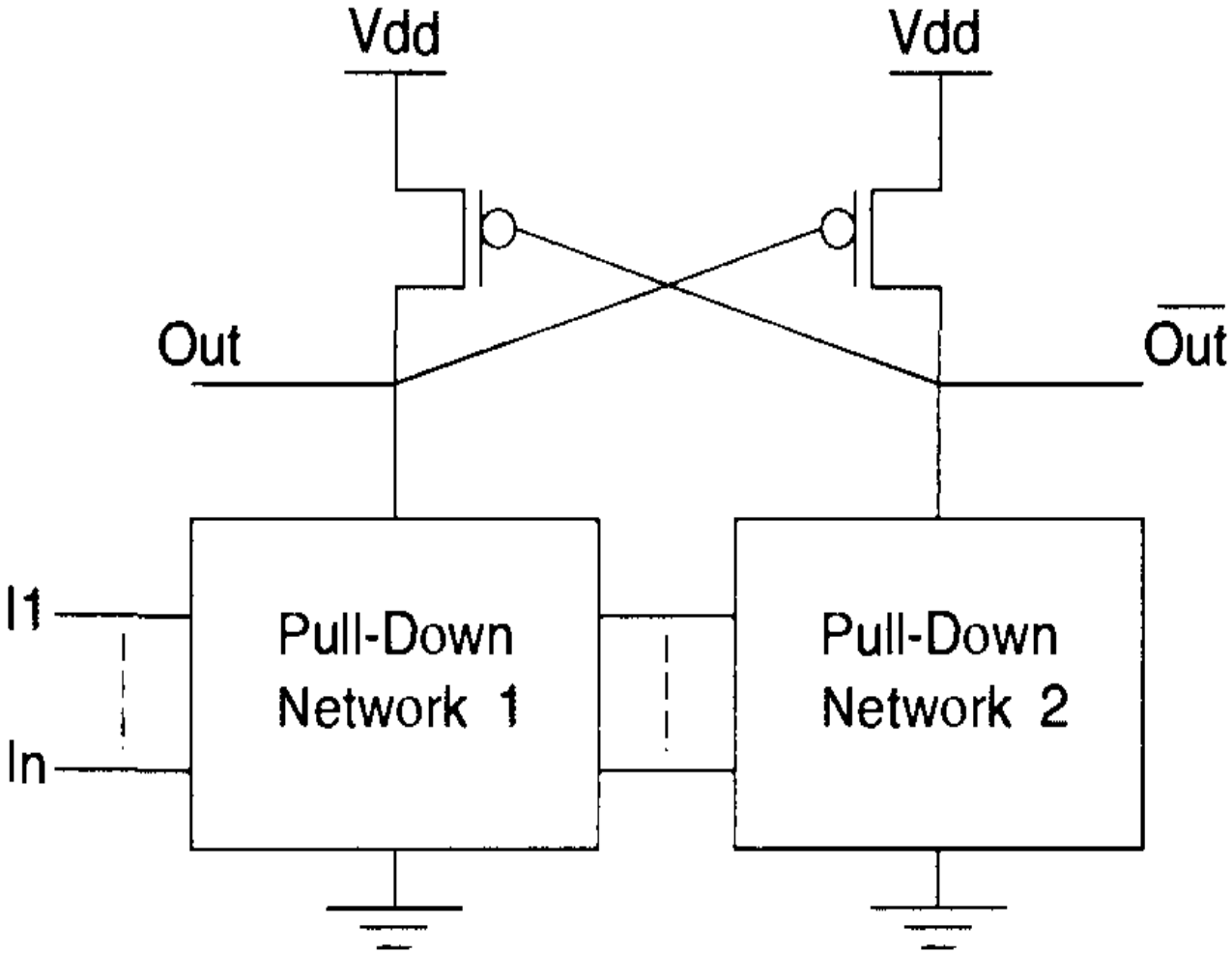
Depletion Load nMOS Logic



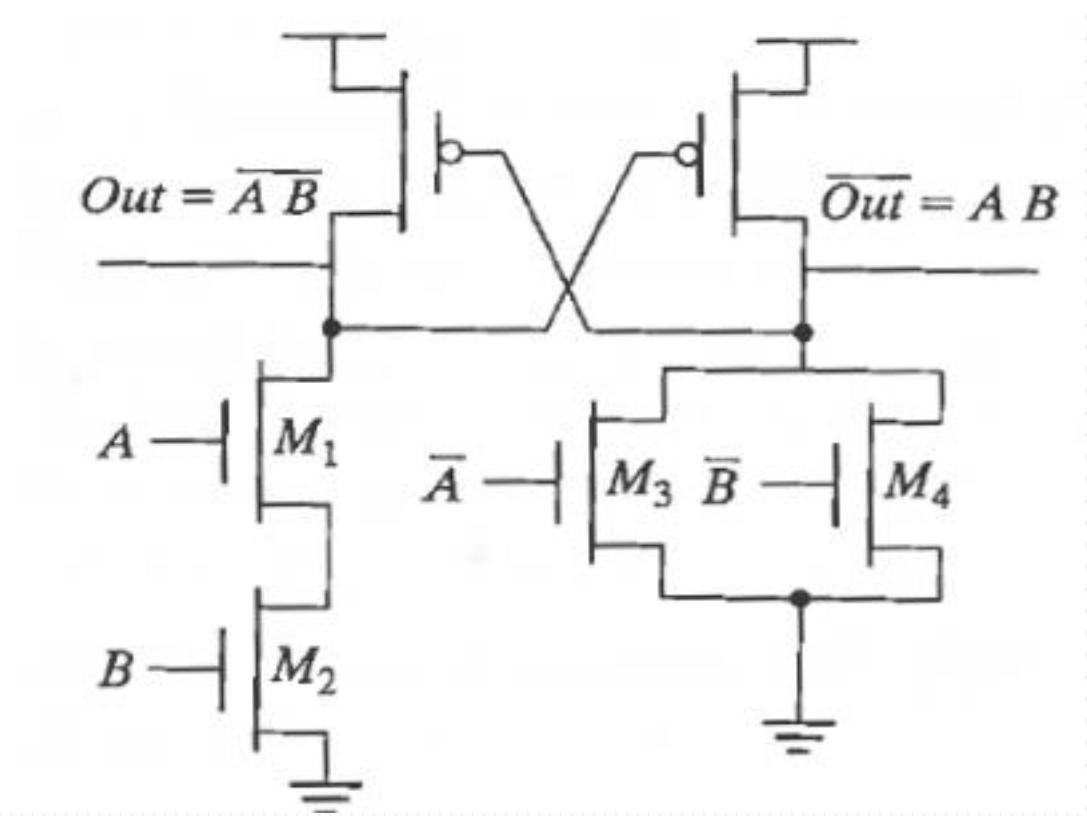
Pseudo nMOS



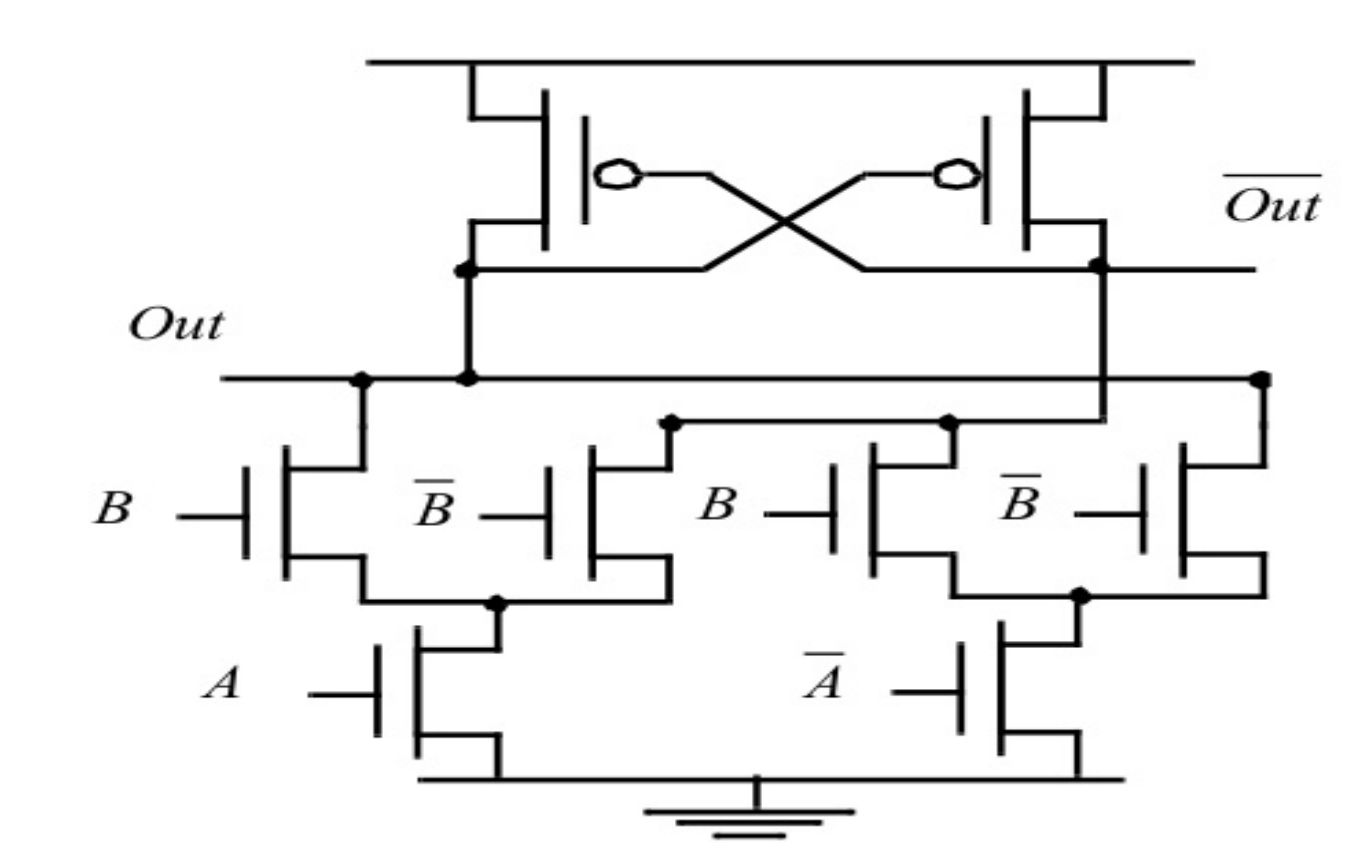
Differential Cascade Voltage Switch Logic (DCVS)



AND/NAND

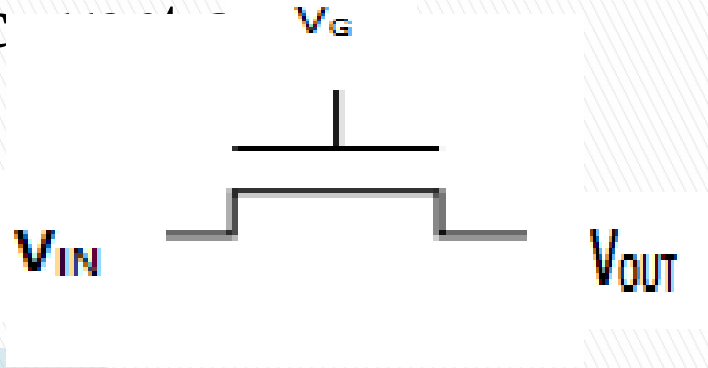

Out = $\overline{A\,B}$
$\overline{Out}$ = A B
A
M_1
$\overline{A}$
M_3
$\overline{B}$
M_4
B
M_2

Ex OR/EX NOR

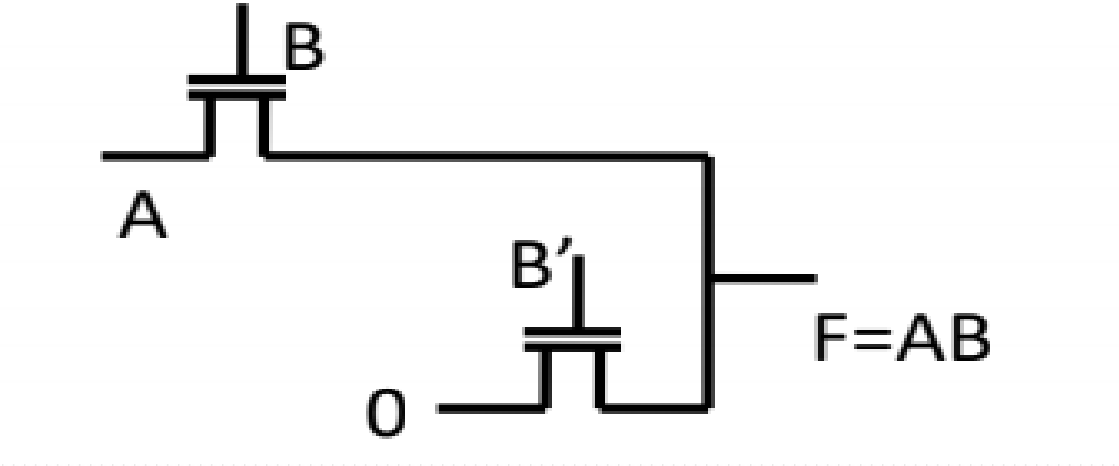


Pass Transistor Logic

- They are simple FETs that pass the signal between the drain and source terminals instead of a fixed power supply value
- The switch is controlled by the gate voltage V_G
- If V_G =0, then the transistor is OFF and there is no connection between the input and output
- Placing a high voltage of $V_G = V_{DD}$ drives the nFET active and c



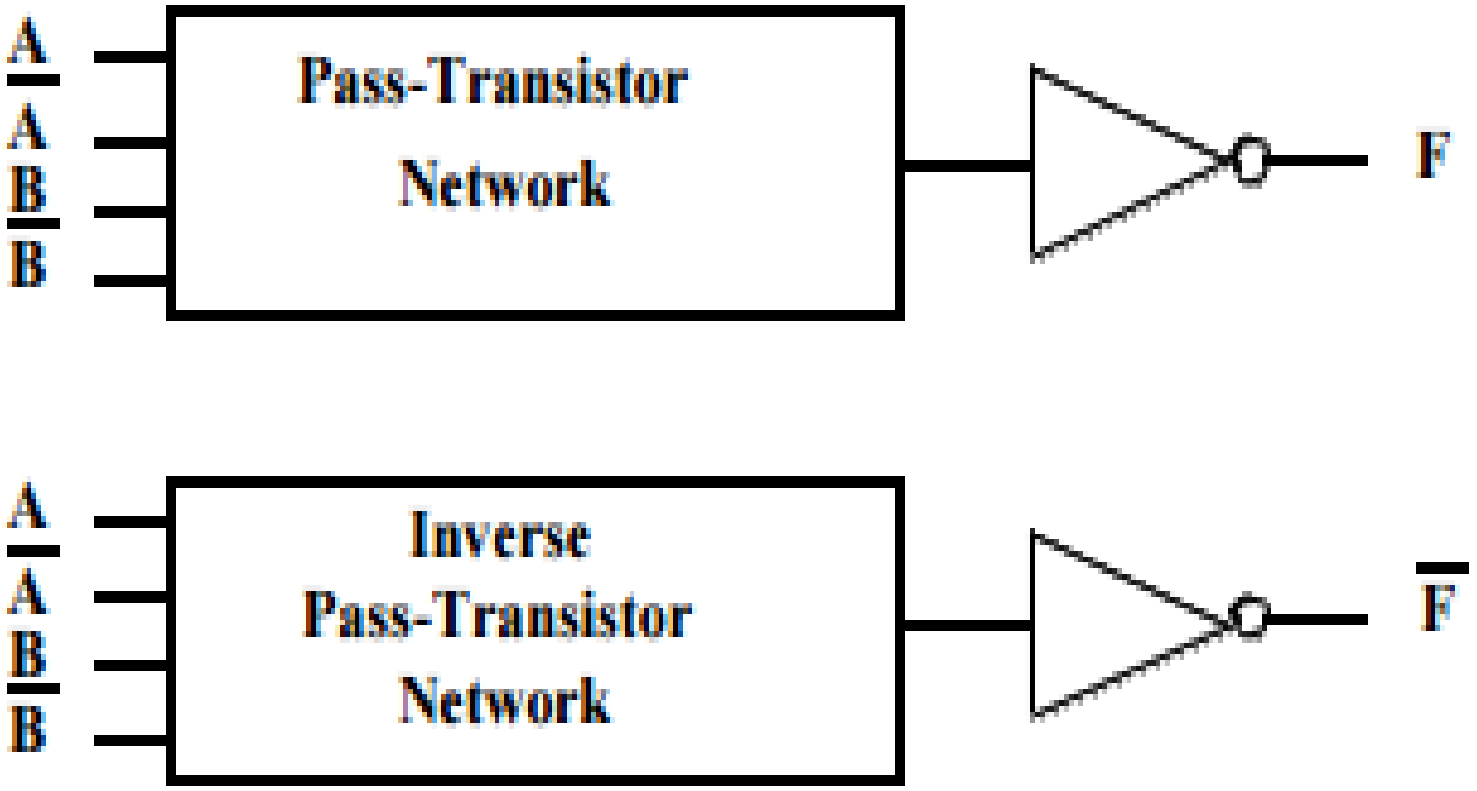
AND implementation



When B=0, F=0
When B=1, F=A

A	B	F
0	0	0
1	0	0
0	1	0
1	1	1

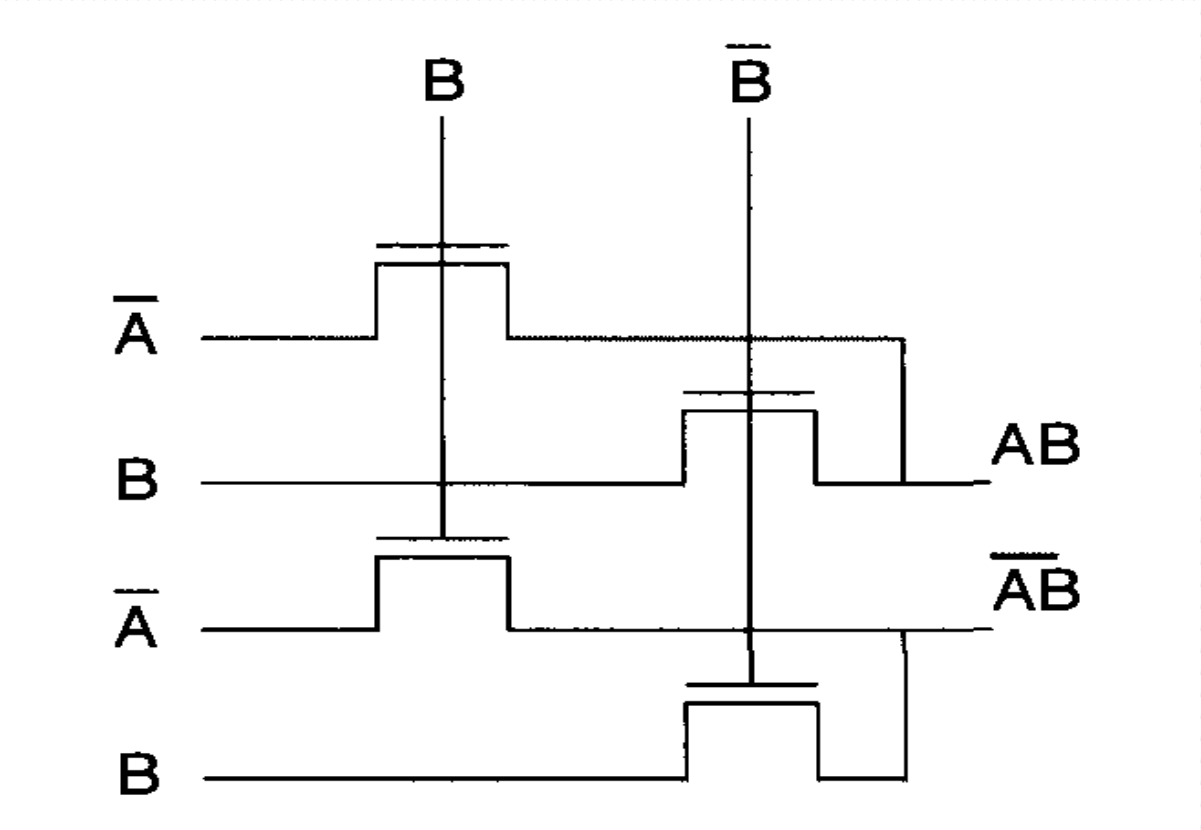
Complementary/ Differntial Pass Transistor Logic (CPL/ DPL)



CPL/ DPL

- Designed for high performance
- Accept true and complementary inputs and produce true and complementary outputs
- Since the circuits are differential complementary data inputs and outputs are always available
- Since circuit is differential, complimentary inputs and outputs are available.
- Although generating differential signals require extra circuitry, complex gates such as XORs, MUXs and adders can be realized efficiently.
- CPL is a static gate, because outputs are connected to V_{DD} or GND through a low-resistance path (high noise resilience).
- Design is modular – all gates use same topology; only inputs are permuted. This facilitates the design of a library of gates

AND/NAND



- Differential pass-transistor logic suffers from the problem of
  - ✓Static power dissipation
  - ✓Reduced noise margin.
- There are several solutions are proposed to deal with such problems-

1. **Level Restoration**
2. **Multiple-Threshold Transistor**
3. **Transmission gate logic**