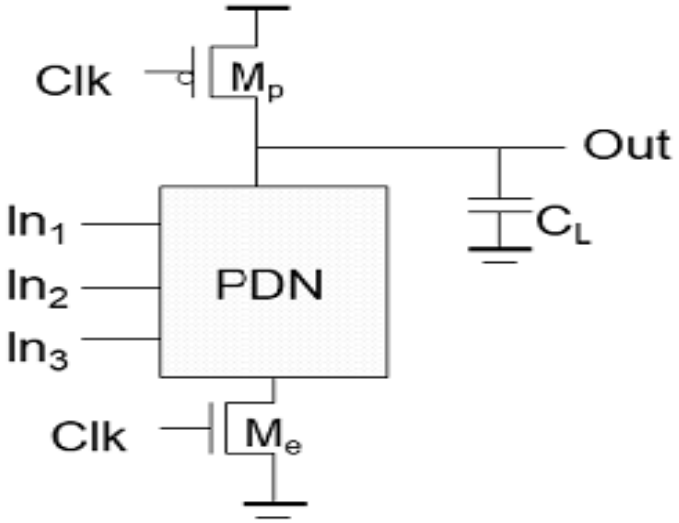
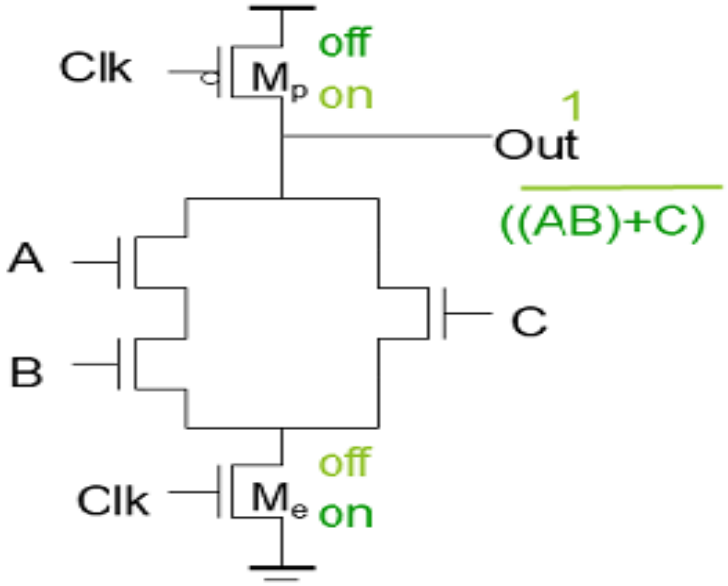
# EC 464 – LPVLSI

## Module IV

# Dynamic Gate

$Out = \overline{CLK} + \overline{((AB)+C)} \cdot CLK$




Two phase operation

Precharge (Clk = 0)

Evaluate (Clk = 1)

- The logic is implemented using N type gates

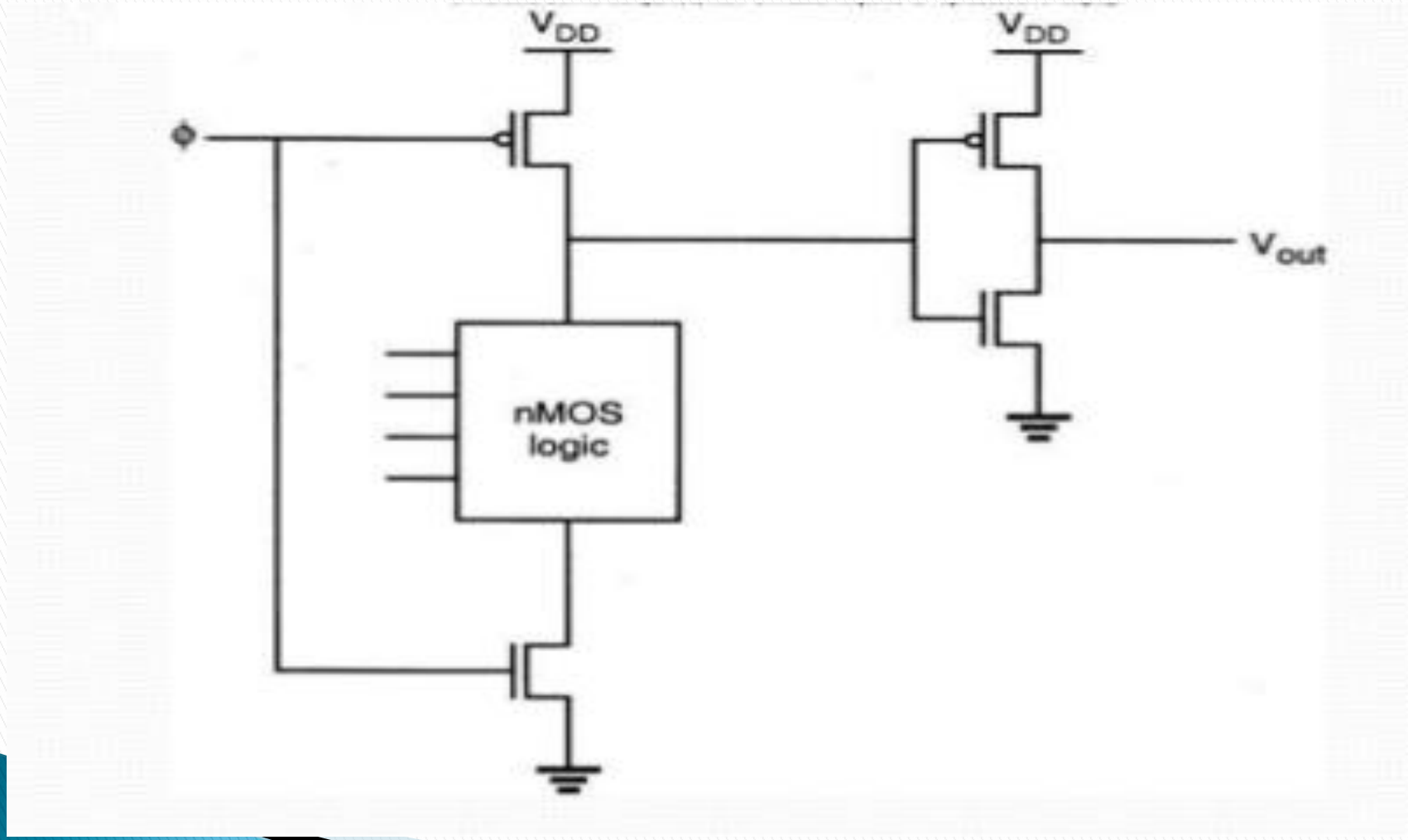
# Precharge phase

- When CLK =0, the output node OUT is precharged to $V_{DD}$ by the PMOS transistor $M_p$
- During that time, nMOS $M_e$ is OFF and the pull down path is disabled
- The input voltages are applied during this phase but they have no influence on the output level since $M_e$ is turned OFF
- The evaluation FET eliminates any static power that would be consumed during the precharge period

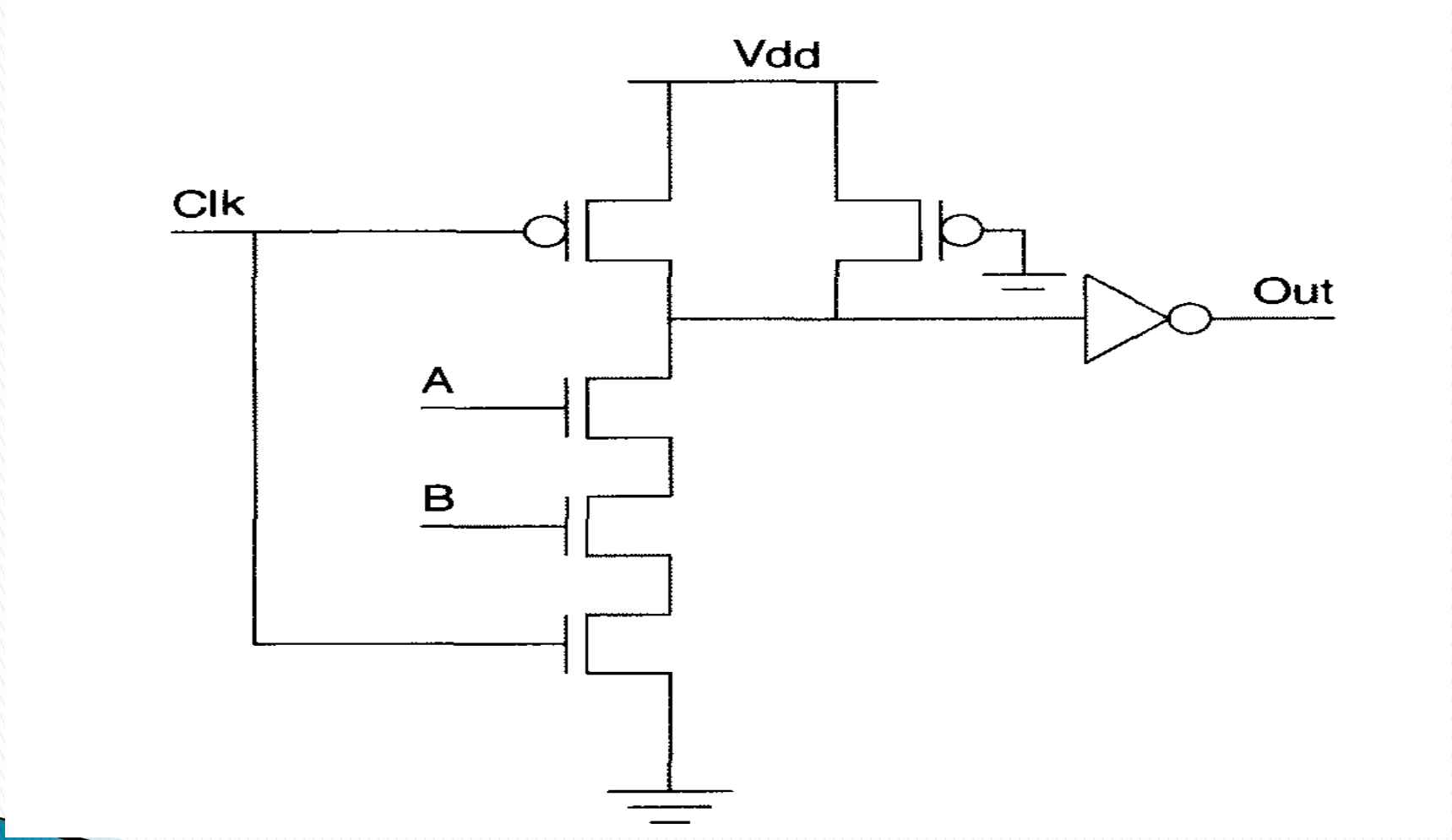
# Evaluation

- When CLK=1, the precharge transistor $M_p$ is turned OFF and the evaluation transistor $M_e$ is turned ON
- The output is conditionally discharged based on the input values and the pull down topology
- If the inputs are such that the PDN conducts, a low resistance path exists between OUT and GND and the output is discharged to ground
- If the PDN is turned OFF, the output value remains at $V_{DD}$ and remains stored on the output capacitance

# Domino logic



# Domino NAND



# Differential Current Switch Logic (DCSL)